# Space Vector Modulation for Three-Phase Six-Switch Dual-Terminal Converter


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***Abstract*— Recently, six-switch dual-terminal inverter (SSDTI) has been proposed as a reduced switch count converter which employs less number of semiconductor devices compared with former dual-terminal inverters proposed so far in the literature. The sinusoidal pulse width modulation (SPWM) is the only switching method which has been presented for this inverter. In this paper a space vector modulation (SVM) switching method is introduced for SSDTI. The proposed SVM method is developed for different frequency (DF) mode of SSDTI operation. Furthermore, different SVM switching patterns are proposed to achieve minimum total harmonic distortion (THD) and minimum number of switching. The performance of the proposed SVM is verified by simulation and experimental results.**



***Keywords*— Reduced switch-count converters, Six-switch Dual-terminal inverter (SSDTI), Space vector modulation (SVM), Different frequency (DF) mode**


## I. INTRODUCTION

Implementing low-cost power inverters has gained traction in power-electronics-based systems especially motor drive systems. Furthermore, in many applications, there is a need for independently supplying two three-phase AC loads. These two objectives have been addressed in the literature by using reduced switch-count dual-terminal inverters (RSCDTI) [1-3]. RSCDTIs employ less number of active switches compared with two B6 inverters, which consists of twelve switches and free-wheeled diodes. In several papers, five-leg inverter and nine-switch inverter (NSI) have been used as RSCDTI [1, 2, 4-9]. As shown in Fig. 1 (a), in five-leg inverter, two phases of each load are separately connected to four legs of the inverter, while one leg is shared between the third phase of the loads [1]. Nine-switch inverter that is shown in Fig. 1 (b) has three legs each composed of three switches. The middle switches $S_{AM}$, $S_{BM}$ and $S_{CM}$ are the joints between the two outputs [2].

Recently six-switch dual-terminal inverter (SSDTI) has been presented for independently controlling two three-phase loads using less number of switches (Fig.2) [3]. SSDTI has also been used as an AC/AC converter in [10-12]. SSDTI has only six active switches and hence its number of switches is reduced by 33 and 40%, respectively, compared with nine-switch and five-leg inverters. A sinusoidal pulse width modulation (SPWM) method for SSDTI has already presented in [3]. In this method, two reference signals (upper and lower) are used for each phase. Gate signals of upper and lower switches are resulted from comparing the carrier signal with upper and lower reference signals, respectively. Gate signals of middle switches are generated by logical XOR of the upper and lower gate signals in each leg. Applying this scheme, there are always two ON switches in each leg.

This paper proposes space vector modulation (SVM) methods for SSDTI. In order to reduce the number of semiconductor switching and minimize the output THD, some specific switching patterns for SVM are also proposed. This paper consists of five sections. Section II describes the carrier based PWM control method for SSDTI. Section III examines the proposed SVM for six-switch dual-terminal inverter. Two special SVM switching patterns with minimum number of switching and minimum THD are presented in section IV. Finally, the validity of performance of the proposed SVM is verified by simulation and experimental results in Section V.

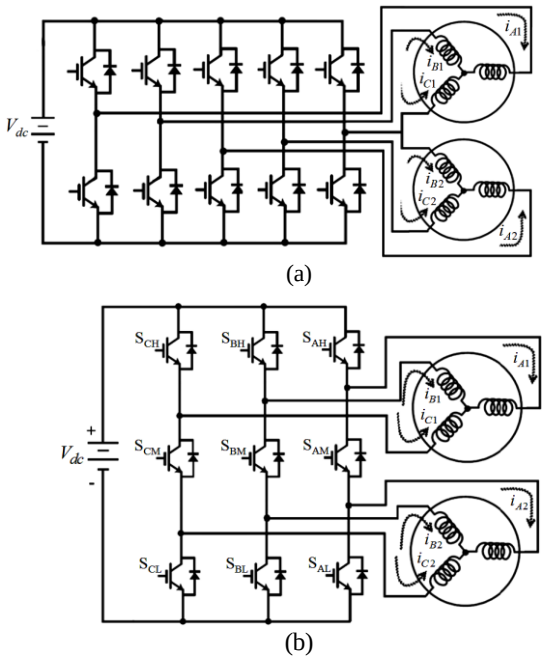



Fig. 1. (a) Five-leg inverter, (b) Nine-switch inverter

## II. SINUSOIDAL PWM SWITCHING METHOD

Fig. 3 illustrates a general six-switch dual-terminal converter (SSDTC) which can be used as inverter or AC/AC converter. In the case of inverter, it is needed to feed the DC link through an extra DC source such as a front-end rectifier for charging the DC-link capacitors. It should be noticed that there is no need to the extra DC source in AC/AC applications since the DC-link capacitors can be charged through one of the AC terminals using appropriate control method. In Fig. 3, voltage levels of DC-link capacitors are considered as a function of three *a*, *b* and *c* coefficients. These coefficients are to be adjusted in a manner to achieve balanced three-phase outputs voltages without DC component.

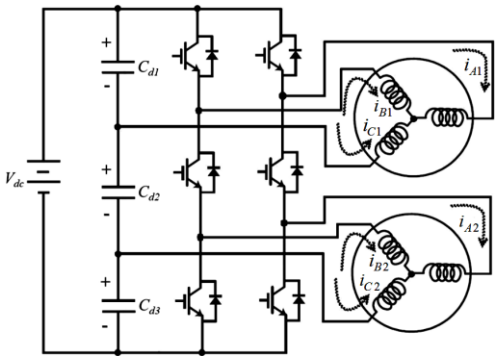



Fig. 2. Dual-terminal six-switch inverter

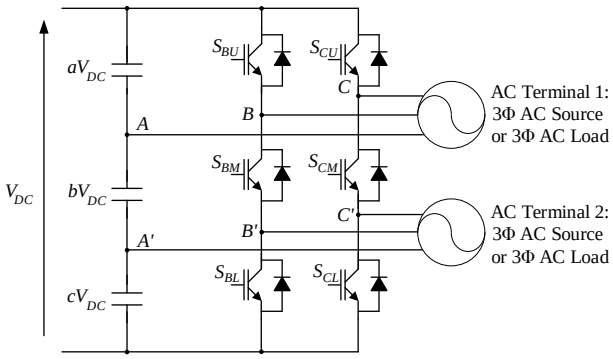



Fig. 3. Genaral six-switch dual-terminal converter

The sinusoidal PWM switching method for six-switch dual-terminal converter is shown in Fig. 4. There are two reference signals (upper and lower) for each leg of converter. The lower reference signal ($V_{refJL}$) which is related to the lower output should not be higher than the upper reference signal ($V_{refJU}$) at any moment. For this reason, the offset value for each reference waveform should be considered to prevent interference between modulating signals [3]. Gate signals of $S_{BU}$ and $S_{CU}$ switches are resulted from comparing $V_{refJU}$ with the carrier signal. Gate signals of $S_{BL}$ and $S_{CL}$ switches are the logical NOT of the values obtained by comparing $V_{refJL}$ with the carrier signal. Gate signals of $S_{BM}$ and $S_{CM}$ are generated by logical XOR of the upper and lower gate signals in each leg. Applying this scheme, in each inverter leg, two switches are always ON. Fig. 5 shows sinusoidal PWM method switching vectors.

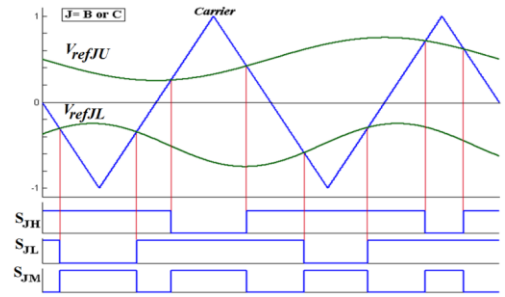



Fig. 4. Sinusoidal PWM method for six-switch dual-terminal converter

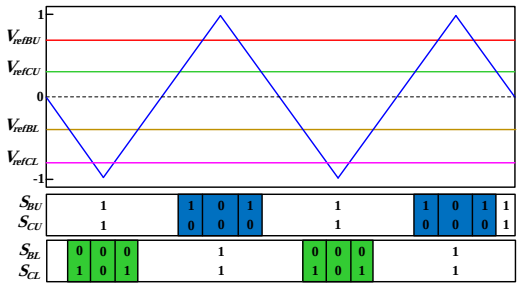



Fig. 5. Sinusoidal PWM method switching vector

## III. SVM FOR SIX-SWITCH DUAL-TEMINAL CONVERTER

Similar to nine-switch converter SVM method, the proposed SVM for SSDTC is only presented for DF mode. However, in contrast to nine-switch converter, there is no zero vector in SSDTC and when one of the outputs has an active vector, the other output also has another active vector, whereas in nine-switch converter when one of the outputs has an active vector, the other output has long zero vector. Considering this fact, the switching time intervals of vectors will be calculated in the following. As mentioned earlier, two switches are always ON in each inverter leg and as a result the different switching modes of SSDTC will be nine as shown in Fig. 6. Table II shows these nine modes of operation and the corresponding phase voltage of upper and lower terminals in each mode. An inverter leg may be in {1}, {0} or {-1} states. The state of semiconductors in these states is illustrated in Table I where, *J* is *B*, or *C*. Voltage levels of DC-link capacitors are assumed to be $aV_{DC}$, $bV_{DC}$ and $cV_{DC}$ in which $V_{DC}$ is DC-link voltage. The upper ($\bar{V}_U$) and lower ($\bar{V}_L$) space vectors of SSDTC in each switching mode are tabulated in Table III. To determine correct active switches, two space vectors are depicted in complex plane, Fig. 7. The SVM active vectors are determined regarding to location of the lower reference signal ($V_{Lref}$ ) in Fig.7(a) and the upper reference signal ($V_{Uref}$ ) in Fig. 7(b). The reference signals for the upper and lower outputs are defined as:

$$\bar{V}_{ref\,U} = V_{ref\,U} e^{j\alpha_U} \tag{1}$$

$$\bar{V}_{ref\,L} = V_{ref\,L} e^{j\alpha_L} \tag{2}$$

where

$$\alpha_U = 2\pi f_U t + \phi_U \tag{3}$$

$$\alpha_L = 2\pi f_L t + \phi_L \tag{4}$$

Similar to SPWM switching method of SSDTC, the DC-link voltage coefficients *a*, *b* and *c* do not have any impact on phase voltage amplitudes and their values may only result in making DC offset in the output voltages. Therefore, in order to make upper and lower space vectors symmetrical and for more simplicity, it is assumed that coefficient *b* is equal to zero and the coefficients *a* and *c* are equal to 0.5 (in accordance with the relation $a+b+c=1$). Considering this assumption, the symmetrical upper and lower space vectors are depicted in Fig. 8. In this figure, the total area of space diagram is divided to two A and B regions. In this paper, a method for creating reference vectors $\bar{V}_{refU}$ and $\bar{V}_{refL}$ using the upper and lower space vectors is proposed. For this purpose, depending on the location of reference vector (A or B region), a combination of switching vectors of different operation modes is used in a specific sequence to create reference space vectors. If the upper reference vector ($\bar{V}_{refU}$) is in region A, a combination of vectors $V_1$, $V_8$, $V_9$ and $V_5$ is employed. In the case where $\bar{V}_{refU}$ is placed in region B, the vectors $V_1$, $V_9$, $V_6$ and $V_5$ are selected for switching. It should be noticed that when these vectors are applied, their effect should also be considered in the lower terminal of SSDTC. As an instance, using vector $V_1$ in each switching cycle for creating $\bar{V}_{refU}$, according to Fig. 8, will have an effect on $\bar{V}_{refL}$.

The selected switching vectors in each switching cycle with attention to the presence region of $\bar{V}_{refU}$ and $\bar{V}_{refL}$ are tabulated in Table IV. Based on the location of the reference vectors, the correct active vectors are determined according to this table.

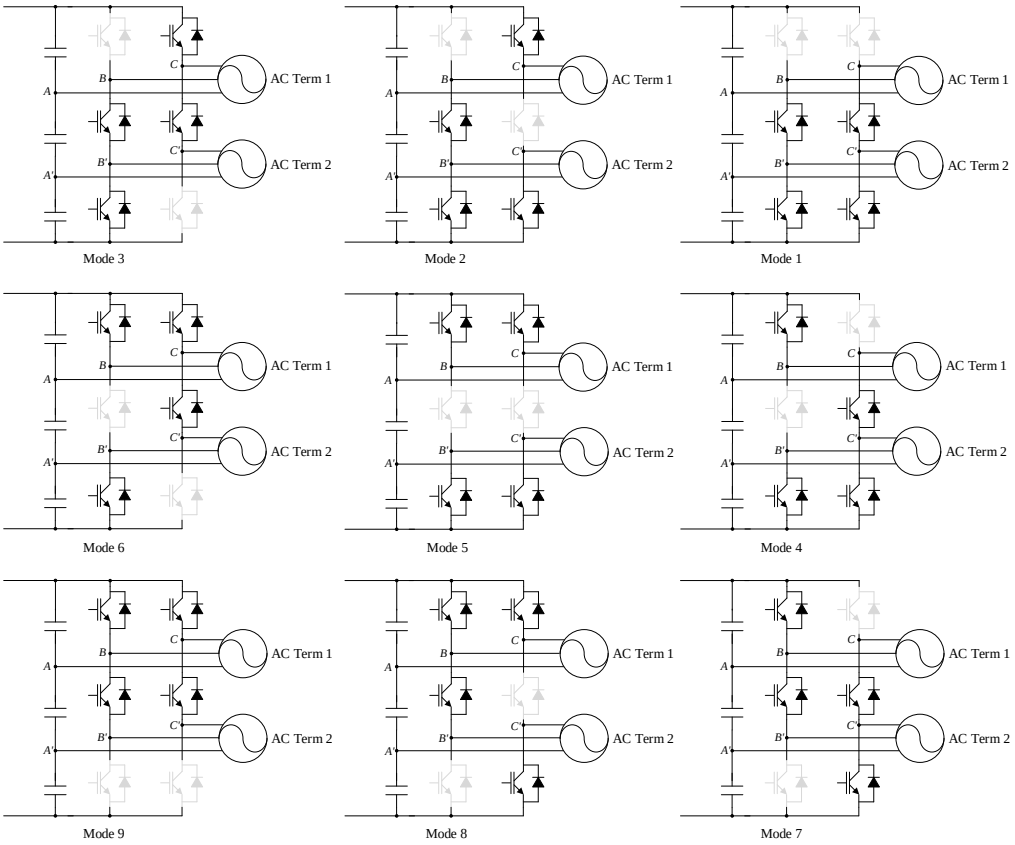



Fig. 6. Different switching modes of SSDTC

TABLE I. STATE OF SWITCHES IN TABLE 1 VECTORS

| | $S_{JU}$ | $S_{JM}$ | $S_{JL}$ |
|---|---|---|---|
| **1** | **ON** | **OFF** | **ON** |
| **0** | **OFF** | **ON** | **ON** |
| **-1** | **ON** | **ON** | **OFF** |

The selected switching vectors in each switching cycle with attention to the presence region of $\bar{V}_{refU}$ and $\bar{V}_{refL}$ are tabulated in Table IV. Based on the location of the reference vectors, the correct active vectors are determined according to Table IV.

If it is assumed that both $\bar{V}_{refU}$ and $\bar{V}_{refL}$ are placed in region A, the switching time intervals of vectors are calculated as:

$$V_{refU}\cos\alpha_U = \frac{1}{T_C}\left[t_1\left(\frac{V_{DC}}{3}\right) - t_9\left(\frac{V_{DC}}{3}\right) - t_8\left(\frac{V_{DC}}{3}\right) - t_5\left(\frac{V_{DC}}{3}\right)\right] \tag{5}$$

$$V_{refU}\sin\alpha_U = \frac{t_4}{T_C}\left(\frac{\sqrt{3}}{3}V_{dc}\right) \tag{6}$$

$$V_{refL}\cos\alpha_L = \frac{1}{T_C}\left[t_1\left(\frac{V_{DC}}{3}\right) + t_4\left(\frac{V_{DC}}{3}\right) - t_9\left(\frac{V_{DC}}{3}\right) + t_5\left(\frac{V_{DC}}{3}\right)\right] \tag{7}$$

$$V_{refL}\sin\alpha_L = \frac{t_8}{T_C}\left(\frac{\sqrt{3}}{3}V_{dc}\right) \tag{8}$$

where, $t_1$, $t_4$, $t_8$, $t_9$ and $t_5$ are, respectively, the time intervals of vectors $V_1$, $V_4$, $V_8$, $V_9$ and $V_5$ and $T_C$ is switching period.

According to aforementioned equations, the value of time intervals of active vectors can be obtained as:

$$t_5 = T_C - t_1 - t_4 - t_9 - t_8 \tag{9}$$

$$t_1 = T_C\left(\frac{3}{\pi}\hat{m}_U\cos\alpha_U + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_U\sin\alpha_U\right) \tag{10}$$

$$t_4 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_U\sin\alpha_U\right) \tag{11}$$

$$t_9 = T_C\left(-\frac{3}{\pi}\hat{m}_L\cos\alpha_L + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_L\sin\alpha_L\right) \tag{12}$$

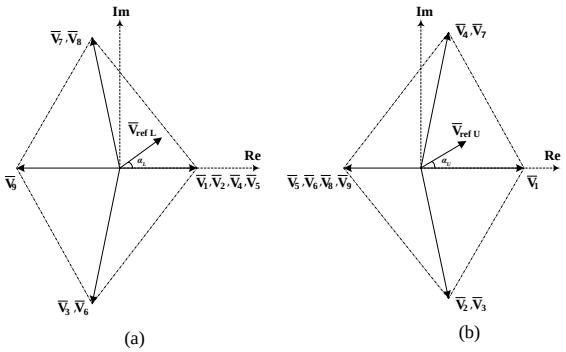
$$t_8 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_L\sin\alpha_L\right) \tag{13}$$

$\hat{m}_U$ and $\hat{m}_L$ are modified modulation indices and defined by:

$$\hat{m}_U = \frac{V_{refU}}{\hat{V}_{1sw}} \tag{14}$$

$$\hat{m}_L = \frac{V_{refL}}{\hat{V}_{1sw}} \tag{15}$$

where $\hat{V}_{1sw}$ is the amplitude of fundamental component of square wave voltage in B6 inverter which is equal to $2V_{DC}/\pi$.




(a) (b)

Fig. 7. Space vector diagrams for SSDTC: a) Lower output, b) Upper output

TABLE II. SWITCHING VCTORS OF SSDTC AND THE CORRESPONDING PHASE VOLTAGE OF UPPER AND LOWER TERMINALS

| Vector | Leg B | Leg C | $V_{AU}$ | $V_{BU}$ | $V_{CU}$ | $V_{AL}$ | $V_{BL}$ | $V_{CL}$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | $2(b+c)V_{DC}/3$ | $-(b+c)V_{DC}/3$ | $-(b+c)V_{DC}/3$ | $2cV_{DC}/3$ | $-cV_{DC}/3$ | $-cV_{DC}/3$ |
| 2 | 0 | 1 | $(-a+b+c)V_{DC}/3$ | $(-a-2b-2c)V_{DC}/3$ | $(2a+b+c)V_{DC}/3$ | $2cV_{DC}/3$ | $-cV_{DC}/3$ | $-cV_{DC}/3$ |
| 3 | 0 | -1 | $(-a+b+c)V_{DC}/3$ | $(-a-2b-2c)V_{DC}/3$ | $(2a+b+c)V_{DC}/3$ | $(-a-b+c)V_{DC}/3$ | $(-a-b-2c)V_{DC}/3$ | $(2a+2b+c)V_{DC}/3$ |
| 4 | 1 | 0 | $(-a+b+c)V_{DC}/3$ | $(2a+b+c)V_{DC}/3$ | $(-a-2b-2c)V_{DC}/3$ | $2cV_{DC}/3$ | $-cV_{DC}/3$ | $-cV_{DC}/3$ |
| 5 | 1 | 1 | $-2aV_{DC}/3$ | $aV_{DC}/3$ | $aV_{DC}/3$ | $2cV_{DC}/3$ | $-cV_{DC}/3$ | $-cV_{DC}/3$ |
| 6 | 1 | -1 | $-2aV_{DC}/3$ | $aV_{DC}/3$ | $aV_{DC}/3$ | $(-a-b+c)V_{DC}/3$ | $(-a-b-2c)V_{DC}/3$ | $(2a+2b+c)V_{DC}/3$ |
| 7 | -1 | 0 | $(-a+b+c)V_{DC}/3$ | $(2a+b+c)V_{DC}/3$ | $(-a-2b-2c)V_{DC}/3$ | $(-a-b+c)V_{DC}/3$ | $(2a+2b+c)V_{DC}/3$ | $(-a-b-2c)V_{DC}/3$ |
| 8 | -1 | 1 | $-2aV_{DC}/3$ | $aV_{DC}/3$ | $aV_{DC}/3$ | $(-a-b+c)V_{DC}/3$ | $(2a+2b+c)V_{DC}/3$ | $(-a-b-2c)V_{DC}/3$ |
| 9 | -1 | -1 | $(a+b)V_{DC}/3$ | $aV_{DC}/3$ | $aV_{DC}/3$ | $-2(a+b)V_{DC}/3$ | $(a+b)V_{DC}/3$ | $(a+b)V_{DC}/3$ |

TABLE III. DIFFERENT SWITCHING MODES OF SSDTC AND UPPER AND LOWER SPACE VECTORS

| Vector | Leg B | Leg C | $\overline{V}_U$ | $\overline{V}_L$ |
|---|---|---|---|---|
| $\overline{V}_1$ | 0 | 0 | $2(b+c)\,V_{DC}/3+0j$ | $2c\,V_{DC}/3+0j$ |
| $\overline{V}_2$ | 0 | 1 | $(-a+b+c)V_{DC}/3-j\sqrt{3}V_{DC}/3$ | $2c\,V_{DC}/3+0j$ |
| $\overline{V}_3$ | 0 | -1 | $(-a+b+c)V_{DC}/3-j\sqrt{3}V_{DC}/3$ | $(-a-b+c)V_{DC}/3-j\sqrt{3}V_{DC}/3$ |
| $\overline{V}_4$ | 1 | 0 | $(-a+b+c)V_{DC}/3+j\sqrt{3}V_{DC}/3$ | $2c\,V_{DC}/3+0j$ |
| $\overline{V}_5$ | 1 | 1 | $-2a\,V_{DC}/3+0j$ | $2c\,V_{DC}/3+0j$ |
| $\overline{V}_6$ | 1 | -1 | $-2a\,V_{DC}/3+0j$ | $(-a-b+c)V_{DC}/3-j\sqrt{3}V_{DC}/3$ |
| $\overline{V}_7$ | -1 | 0 | $(-a+b+c)V_{DC}/3+j\sqrt{3}V_{DC}/3$ | $(-a-b+c)V_{DC}/3+j\sqrt{3}V_{DC}/3$ |
| $\overline{V}_8$ | -1 | 1 | $-2a\,V_{DC}/3+0j$ | $(-a-b+c)V_{DC}/3+j\sqrt{3}V_{DC}/3$ |
| $\overline{V}_9$ | -1 | -1 | $-2a\,V_{DC}/3+0j$ | $-2a\,V_{DC}/3+0j$ |

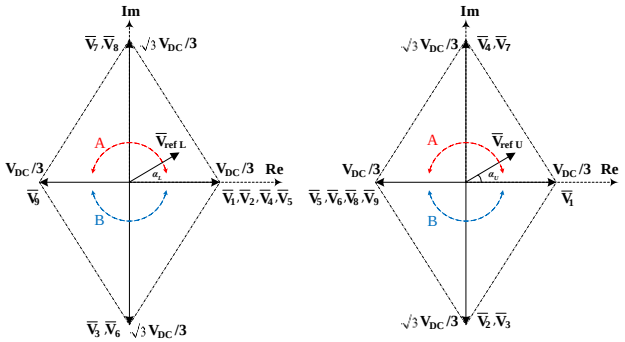



Fig. 8. Space vector diagrams for SSDTC with $a = c = 0.5$, $b = 0$: a) Lower output, b) Upper output

Following the same procedure, the switching time intervals of vectors in other regions can be obtained which are tabulated in Table V. In this table, the value of $\alpha_U$ and $\alpha_L$ should be normalized between 0 and π. Considering the fact that the sum of the time intervals of vectors is less than switching period, the upper and lower modified modulation indices should always fulfill the following criteria:

$$\hat{m}_U \le \frac{\sqrt{3}V_{dc}/12}{2V_{dc}/\pi} = 0.2267 \tag{16}$$

$$\hat{m}_L \le \frac{\sqrt{3}V_{dc}/12}{2V_{dc}/\pi} = 0.2267 \tag{17}$$

Thus, 22.67 percent of $\hat{V}_{1sw}$ in B6 inverter is achieved.

## IV. OPTIMUM SWITCHING VECTOR SEQUENCE

In this section, we try to find optimum SSDTC vector sequences for the proposed SVM. For this purpose, a special

TABLE IV. SWITCHING VECTORS SELECTION BASED ON BASED ON THE LOCATION OF THE REFERENCE VECTOR

| $\overline{V}_{ref\ U}$ | $\overline{V}_{ref\ L}$ | The Selected Switching Vectors in Each Cycle |
|---|---|---|
| Region A $0 \le \alpha_U < \pi$ | Region A $(0 \le \alpha_L < \pi)$ | Mode 1 ($V_1$), Mode 4 ($V_4$), Mode 8 ($V_8$), Mode 9 ($V_9$), Mode 5 ($V_5$) |
| | Region B $(\pi \le \alpha_L < 2\pi$ | Mode 1 ($V_1$), Mode 4 ($V_4$), Mode 6 ($V_6$), Mode 9 ($V_9$), Mode 5 ($V_5$) |
| Region B $\pi \le \alpha_U < 2\pi$ | Region A $0 \le \alpha_L < \pi)$ ( | Mode 1 ($V_1$), Mode 2 ($V_2$), Mode 8 ($V_8$), Mode 9 ($V_9$), Mode 5 ($V_5$) |
| | Region B $(\pi \le \alpha_L < 2\pi)$ | Mode 1 ($V_1$), Mode 2 ($V_2$), Mode 6 ($V_6$), Mode 9 ($V_9$), Mode 5 ($V_5$) |

switching vector sequence is presented in Fig. 9(a). This switching sequence reduces the number of semiconductor switching and as a result decreases the switching loss. In this method, vector $V_5$ is placed between other active vectors during each switching cycle. Thus, when the legs status changes form {1,0} or {0,1} to {-1,1} or {1,-1}, vector $V_5$ ({1,1}) is used in order to minimum the number of switching.

Fig. 9(b) shows another special sequence of switching vectors which results in low output voltage THD. To achieve this objective, the combination of switching vectors is chosen so that vector $V_5$ is placed between $V_1$, $V_2$ or $V_1$, $V_4$ and also between $V_8$, $V_9$ or $V_6$, $V_9$ to make the switching pattern symmetrical. As shown in Fig. 9(b), each group of symmetrical vectors is placed in one side of the switching pattern which makes the whole switching cycle asymmetric. To overcome this problem and make the cycle symmetrical, another specific switching sequence is proposed as reflected in Fig. 9(c). First, the vectors $V_1$, $V_2$ or $V_1$, $V_4$ are used, then $V_9$, $V_8$ or $V_9$, $V_6$ are employed

TABLE V. SWITCHING VECTORS SELECTION BASED ON BASED ON THE LOCATION OF THE REFERENCE VECTOR

| $\overline{V}_{ref\ U}$ | $\overline{V}_{ref\ L}$ | Switching Time Intervals of Vectors in One Cycle |
|---|---|---|
| **Region A** $0 \le \alpha_U < \pi$ | **Region A** $0 \le \alpha_L < \pi$ | $t_1 = T_C\left(\frac{3}{\pi}\hat{m}_U \cos\alpha_U + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_4 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_9 = T_C\left(-\frac{3}{\pi}\hat{m}_L \cos\alpha_L + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_8 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_5 = T_C - t_1 - t_4 - t_9 - t_8$ |
| | **Region B** $\pi \le \alpha_L < 2\pi$ | $t_1 = T_C\left(\frac{3}{\pi}\hat{m}_U \cos\alpha_U + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_4 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_9 = T_C\left(\frac{3}{\pi}\hat{m}_L \cos\alpha_L + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_6 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_5 = T_C - t_1 - t_4 - t_9 - t_6$ |
| **Region B** $\pi \le \alpha_U < 2\pi$ | **Region A** $0 \le \alpha_L < \pi$ | $t_1 = T_C\left(-\frac{3}{\pi}\hat{m}_U \cos\alpha_U + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_2 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_9 = T_C\left(-\frac{3}{\pi}\hat{m}_L \cos\alpha_L + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_8 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_5 = T_C - t_1 - t_2 - t_9 - t_8$ |
| | **Region B** $\pi \le \alpha_L < 2\pi$ | $t_1 = T_C\left(\frac{3}{\pi}\hat{m}_U \cos\alpha_U + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_2 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_U \sin\alpha_U\right)$<br>$t_9 = T_C\left(-\frac{3}{\pi}\hat{m}_L \cos\alpha_L + \frac{1}{2} - \frac{\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_6 = T_C\left(\frac{2\sqrt{3}}{\pi}\hat{m}_L \sin\alpha_L\right)$<br>$t_5 = T_C - t_1 - t_2 - t_9 - t_6$ |

TABLE VI. THE NUMBER OF SWITCHING PER CYCLE IN DIFFERENT METHODS

| SVM (Minimum THD) | SVM (Low THD) | SVM (Minimum Switching) | SPWM |
|---|---|---|---|
| **26** | **24** | **12** | **16** |

TABLE VII. SIMULATION AND EXPERIMENTAL RESULTS

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_{DC}$ | 208 V | $f_U$ | 50 Hz |
| $R$ | 5 Ohm | $f_L$ | 60 Hz |
| $L$ | 6 mH | Switching Frequency | 6 kHz |
| $R'$ | 7 Ohm | $\hat{m}_U$ (SVM) | 0.2267 |
| $L'$ | 5 mH | $\hat{m}_L$ (SVM) | 0.17 |

and finally the inverse of these two vector sets are applied. Although this procedure leads to the minimum THD, it increases the number of switching. Table VI shows the number of switching per cycle in different switching method.

## V. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the performance and the validity of the proposed SVMs are investigated by simulation and experimental results. The prototype of the proposed system is shown in Fig. 10. Two resistive-inductive loads are connected to the outputs of SSDTI. The control scheme has been implemented on a TMS320F2812 DSP. Simulation and experimental parameters are listed in Table VII.

Figs. 11 and 12 show simulation and experimental waveforms of the line voltages and currents of both terminals, respectively, when the proposed SVM with minimum switching is used. It should be noticed that since simulation and experimental waveforms of the line voltages and currents for the other two proposed SVM (low THD and minimum THD) resemble Figs. 11 and 12, to avoid verbiage, the simulation and experimental results are discussed here only for the proposed SVM with minimum switching. As is reflected in the Figs. 11 and 12, the frequency and amplitude of the waveform are at the expected values and the current waveform are balanced without DC component thus the proposed SVM method is able to control SSDTC correctly. The DC link capacitor voltages with SVM method are shown in Fig. 13. It can be seen that voltages have settled at the anticipated levels with no extra control mechanism.

The THDs of the output currents against modulation indices with different proposed SVM sequences are displayed in Fig. 14(a). This figure also includes the output THD with SPWM method for better illustration of output waveform characteristics. As is reflected in the figure and was expected, the SVM method with minimum THD has the lowest THD among switching methods. The SPWM and SVM with minimum switching have similar THDs, whereas the THD of the SVM with low THD is less. Fig. 14(b) illustrates the efficiency of the different switching method. As it can be seen in the figure, the SVM with minimum switching method has the highest efficiency in comparison with other methods. SPWM method is ranked second and SVM with low THD and minimum THD are reached third and fourth, respectively.

## VI. CONCLUSION

The novel Space Vector Modulation (SVM) for six-switch dual-terminal inverter (SSDTC) was proposed in this paper. Since there are no zero vectors in SSDTC and when one of the outputs has an active vector, the other output also has another

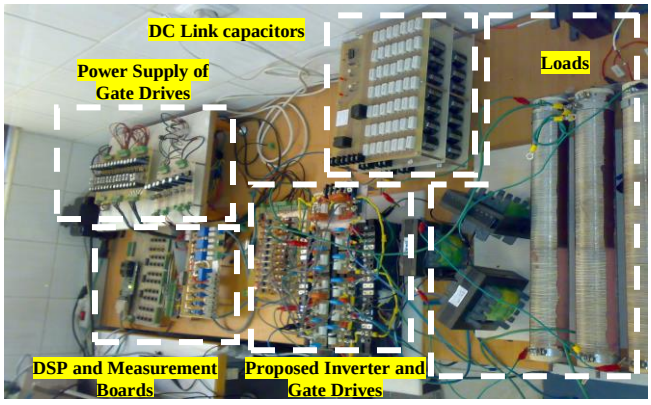



Fig. 10 Prototype of the proposed system

| $\overline{V}_{ref\,U}$ in A | | | $\overline{V}_{ref\,L}$ in A | |
|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_4$ | $\overline{V}_5$ | $\overline{V}_8$ | $\overline{V}_9$ |
| $t_1$ | $t_4$ | $t_5$ | $t_8$ | $t_9$ |

| $\overline{V}_{ref\,U}$ in A | | | $\overline{V}_{ref\,L}$ in B | |
|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_4$ | $\overline{V}_5$ | $\overline{V}_6$ | $\overline{V}_9$ |
| $t_1$ | $t_4$ | $t_5$ | $t_6$ | $t_9$ |

| $\overline{V}_{ref\,U}$ in B | | | $\overline{V}_{ref\,L}$ in A | |
|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_2$ | $\overline{V}_5$ | $\overline{V}_8$ | $\overline{V}_9$ |
| $t_1$ | $t_2$ | $t_5$ | $t_8$ | $t_9$ |

| $\overline{V}_{ref\,U}$ in B | | | $\overline{V}_{ref\,L}$ in B | |
|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_2$ | $\overline{V}_5$ | $\overline{V}_6$ | $\overline{V}_9$ |
| $t_1$ | $t_2$ | $t_5$ | $t_6$ | $t_9$ |

(a)

| $\overline{V}_{ref\,U}$ in A | | | | $\overline{V}_{ref\,L}$ in A | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_4$ | $\overline{V}_5$ | $\overline{V}_4$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_8$ | $\overline{V}_5$ | $\overline{V}_8$ | $\overline{V}_9$ |
| $t_1/2$ | $t_4/2$ | $t_5/2$ | $t_4/2$ | $t_1/2$ | $t_9/2$ | $t_8/2$ | $t_5/2$ | $t_8/2$ | $t_9/2$ |

| $\overline{V}_{ref\,U}$ in A | | | | $\overline{V}_{ref\,L}$ in B | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_4$ | $\overline{V}_5$ | $\overline{V}_4$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_6$ | $\overline{V}_5$ | $\overline{V}_6$ | $\overline{V}_9$ |
| $t_1/2$ | $t_4/2$ | $t_5/2$ | $t_4/2$ | $t_1/2$ | $t_9/2$ | $t_6/2$ | $t_5/2$ | $t_6/2$ | $t_9/2$ |

| $\overline{V}_{ref\,U}$ in B | | | | $\overline{V}_{ref\,L}$ in A | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_2$ | $\overline{V}_5$ | $\overline{V}_2$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_8$ | $\overline{V}_5$ | $\overline{V}_8$ | $\overline{V}_9$ |
| $t_1/2$ | $t_2/2$ | $t_5/2$ | $t_2/2$ | $t_1/2$ | $t_9/2$ | $t_8/2$ | $t_5/2$ | $t_8/2$ | $t_9/2$ |

| $\overline{V}_{ref\,U}$ in B | | | | $\overline{V}_{ref\,L}$ in B | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_2$ | $\overline{V}_5$ | $\overline{V}_2$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_6$ | $\overline{V}_5$ | $\overline{V}_6$ | $\overline{V}_9$ |
| $t_1/2$ | $t_2/2$ | $t_5/2$ | $t_2/2$ | $t_1/2$ | $t_9/2$ | $t_6/2$ | $t_5/2$ | $t_6/2$ | $t_9/2$ |

(b)

| $\overline{V}_{ref\,U}$ in A | | | | $\overline{V}_{ref\,L}$ in A | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_4$ | $\overline{V}_5$ | $\overline{V}_4$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_8$ | $\overline{V}_5$ | $\overline{V}_8$ | $\overline{V}_9$ |
| $t_1/2$ | $t_4/2$ | $t_5/2$ | $t_4/2$ | $t_1/2$ | $t_9/2$ | $t_8/2$ | $t_5/2$ | $t_8/2$ | $t_9/2$ |

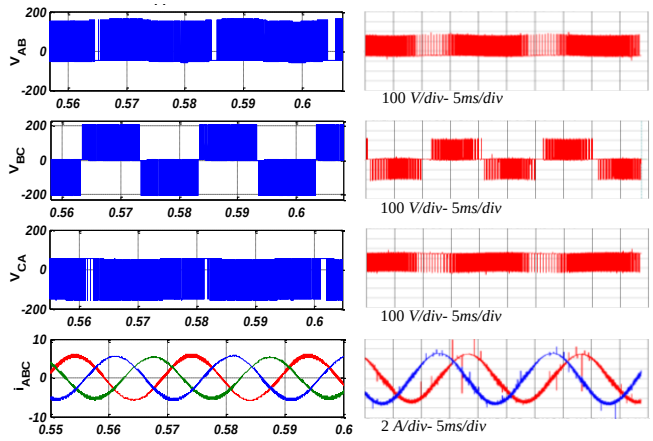
| $\overline{V}_{ref\,U}$ in A | | | | $\overline{V}_{ref\,L}$ in B | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_4$ | $\overline{V}_5$ | $\overline{V}_4$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_6$ | $\overline{V}_5$ | $\overline{V}_6$ | $\overline{V}_9$ |
| $t_1/2$ | $t_4/2$ | $t_5/2$ | $t_4/2$ | $t_1/2$ | $t_9/2$ | $t_6/2$ | $t_5/2$ | $t_6/2$ | $t_9/2$ |

| $\overline{V}_{ref\,U}$ in B | | | | $\overline{V}_{ref\,L}$ in A | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_2$ | $\overline{V}_5$ | $\overline{V}_2$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_8$ | $\overline{V}_5$ | $\overline{V}_8$ | $\overline{V}_9$ |
| $t_1/2$ | $t_2/2$ | $t_5/2$ | $t_2/2$ | $t_1/2$ | $t_9/2$ | $t_8/2$ | $t_5/2$ | $t_8/2$ | $t_9/2$ |

| $\overline{V}_{ref\,U}$ in B | | | | $\overline{V}_{ref\,L}$ in B | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{V}_1$ | $\overline{V}_2$ | $\overline{V}_5$ | $\overline{V}_2$ | $\overline{V}_1$ | $\overline{V}_9$ | $\overline{V}_6$ | $\overline{V}_5$ | $\overline{V}_6$ | $\overline{V}_9$ |
| $t_1/2$ | $t_2/2$ | $t_5/2$ | $t_2/2$ | $t_1/2$ | $t_9/2$ | $t_6/2$ | $t_5/2$ | $t_6/2$ | $t_9/2$ |

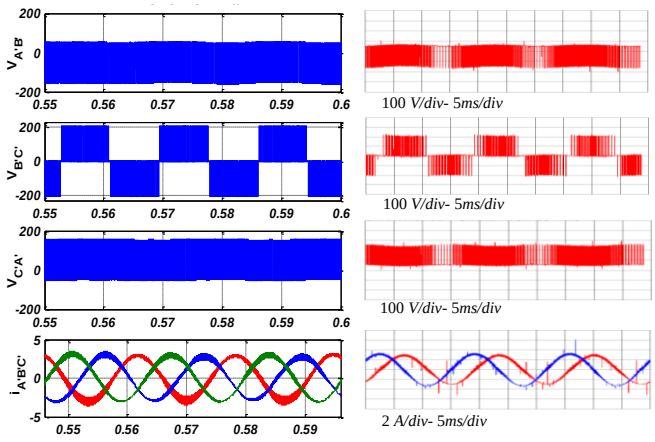
(c)

Fig. 9. Proposed SVM patterns;, (a) with minimum switching, (b) with low THD, (c) with minimum THD




(a) (b)

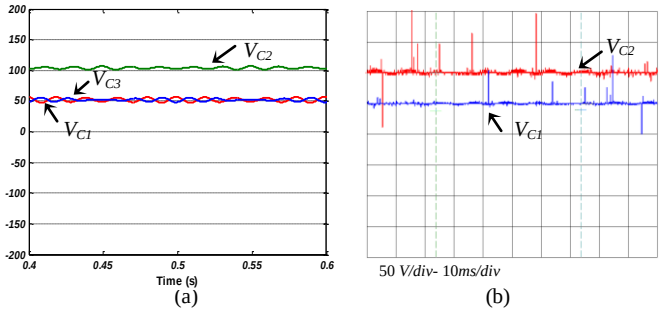
Fig. 11. Upper terminal waveforms, (a) Simulation results, (b) Experimental results




(a) (b)

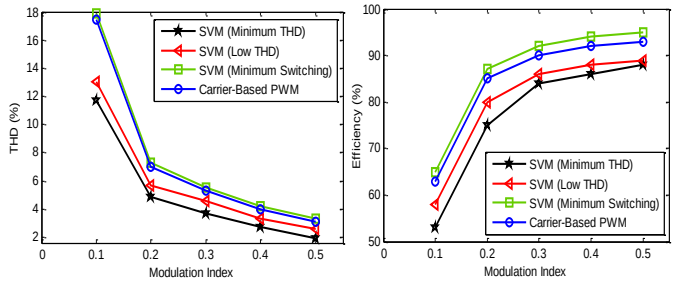
Fig. 12. Lower terminal waveforms, (a) Simulation results, (b) Experimental results

active vector, a specific sequence of vectors is employed to create upper and lower terminals reference vectors. Introducing the proposed SVM and calculating the switching time interval of vectors were developed. Also, a reduced number of semiconductor switching pattern of SVM was proposed. In addition, the SVM with low THD and minimum THD were presented to achieve output waveforms with better THD. The effective operation of the proposed SVM method and different SVM sequences were demonstrated by simulation and confirmed through experimental implementation.




(a) (b)

Fig. 13. DC link capacitors voltage, (a) Simulation results, (b) Experimental results




(a) (b)

Fig. 14. Comparison of different switching method, (a) Efficiency, (b) THD

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