Buck-Boost Reduced Switch-Count Converters based on Three-Phase Six-Switch Dual-Terminal Inverter

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Abstract—**Recently, three-phase six-switch dual-terminal inverter (SSDTI) has been proposed as a reduced switch count converter which employs less number of semiconductor devices compared with former dual-terminal inverters proposed so far in the literature. In SSDTI, the sum of upper and lower modulation indices must be less or equal to one. Therefore, the voltage amplitude of the outputs is small compared to two separate inverters. To remedy this problem, this paper proposes three new buck-boost DC/AC converters based on SSDTI: CUK-SSDTI, SEPIC-SSDTI and Diode-Assisted SSDTI. The performance of the proposed step-up DC/AC converters is verified by simulation and experimental results.**

Keywords— Reduced switch-count converters, Six-switch dual-terminal inverter (SSDTI), Buck-Boost DC/AC converter, CUK-source inverter, SEPIC-source inverter, Diode-Assisted source inverter

III. INTRODUCTION

In many applications, it is required to independently control two or more three-phase AC loads. The conventional solution for this problem is using several separate inverters which increases the cost and volume of the system. Various reduced switch-count multi-terminal inverters (RSCMTI) have been proposed so far for solving this problem [1-5].RSCMTIs employ less number of active switches compared with several conventional inverters. In [1] and [2], five-leg dual-terminal inverter (Fig. 1(a)) and a nine-switch dual-terminal inverter (Fig. 1(b)) are proposed which are employed to independently supply and control two three-phase loads and hence the number of their switches is reduced by 16% and 25%, respectively, compared with two conventional inverters.

Recently six-switch dual-terminal inverter (SSDTI) has been presented for independently controlling two three-phase loads using less number of switches (Fig.2) [3]. As the name shows, SSDTI has only six active switches and hence its number of switches is reduced by 33 and 40%, respectively, compared with nine-switch and five-leg inverters. SSDTI has also been used as an AC/AC converter in [6, 7].In a SSDTI, the sum of the upper and lower modulation indices must be less or equal to one. Therefore, voltage amplitude of outputs is small compared to two separate inverters [3]. For applications like renewable energy harnessing, where the input voltage fluctuates over a wide range, a buck-boost inverter is required to stabilize the AC output voltage at a desired value. To achieve this, there is a need to use a step-up DC/DC converter as front-end of SSDTI.

The bidirectional non-isolated buck-boost inverters are typically (popularly) derived from DC/DC CUK and SEPIC converter as front-end stage of voltage source inverters. Another non-isolated buck-boost inverter proposed in the literature is Z-source converter that utilizes special X shape impedance networks on its dc side [8]. Regardless of advantages of using impedance network like protection against short circuit of DC link, this converter adds some extra passive elements to the system that it can increase the volume and cost. In addition to topological compactness and economic cost, a second factor of concern is the actual physical gain that can be produced by a particular buck–boost inverter topology. [9] proposes a unique X-shaped diode–capacitor network inserted between the inverter circuit and dc source for producing a voltage gain that is comparatively higher than those of CUK and SEPIC converters. This converter is called Diode-Assisted inverter.

With attention to special configuration of SSDTI, this paper proposes three new buck-boost inverters: CUK-SSDTI, SEPIC-SSDTI and Diode-Assisted SSDTI. To do so, a step-up DC/DC converter is placed between DC link source and DC input of SSDTI in a way that in addition to boosting the DC voltage, the output AC waveforms still remain balanced and sinusoidal. The combination of aforementioned DC/DC converters with SSDTI needs some changes in DC-link capacitors configuration.

This paper consists of four sections. Section II of this paper explains operation of six-switch dual-terminal inverter (SSDTI). The topology of the proposed buck-boost inverters, their operational principles and switching algorithms in continuous conduction mode are described in section III. Finally, the validity of performance of the proposed converters is verified by simulation and experimental results in Section IV.

IV. SIX-SWITCH DUAL-TERMINAL INVERTER (SSDTI)

Fig. 1 illustrates a six-switch dual-terminal inverter (SSDTI). A SSDTI can be considered as two separate B4 inverters with two common switches, therefore a special PWM switching technique is needed to independently control two three-phase terminals separately (Fig.2). This technique requires two reference signals (V_{refJU} & V_{refJL}) for each phase legs which are related to upper and lower terminals respectively. These signals are expressed by:

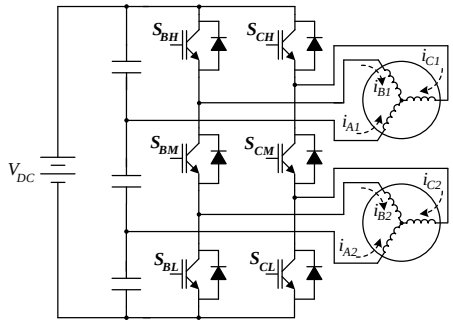


Fig. 1. Dual-terminal six-switch inverter

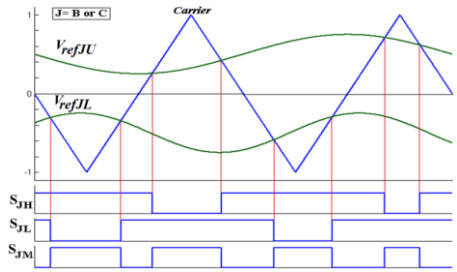


Fig. 2. Sinusoidal PWM method for SSDTI

$$V_{refJU} = m_U \sin(2\pi f_U t + \varphi_{JU}) + Offset_U \quad (1)$$

$$V_{refJL} = m_L \sin(2\pi f_L t + \varphi_{JL}) + Offset_L \quad (2)$$

where m_x and f_x (x = U, L) are, respectively, the reference amplitude and the frequency of the inverter outputs and $Offset_x$ and φ_{Jx} are, respectively, the offset of the modulation signals and phase difference between the phases, and U and L indices refer to upper and lower outputs.

The lower reference signal (V_{refJL}) which is related to the lower output should not be higher than the upper reference signal (V_{refJU}) at any moment. $Offset_U$ and $Offset_L$ are used to prevent interference between upper and lower modulating signals [3]. The gate signal for upper switch of each leg is positive logic value generated by V_{refJU} and carrier waveform. The gate signal for lower switch of each leg is negative logic value generated by V_{refJL} and carrier waveform. The gate signal for middle switches is generated by the logical XOR value of the gate signals for upper and lower switches.

II. Proposed Topologies and Operational Principles

A. CUK-SSDTI Buck-Boost Converter

The proposed CUK-SSDTI buck-boost converter has derived from developing of a single stage CUK converter behind SSDTI. It is shown in Fig. 3 that the converter uses an extra capacitor, an extra inductor and an extra active switch compared with SSDTI. To properly operation of this converter, it is needed to control SW and S_{JH}, S_{JM}, S_{JL} (J=B, C) in a manner that, in addition to creating sinusoidal three phase waveforms in the output, the required boost voltage gain with minimum voltage stress on switches cab be obtained.

The developed modulation scheme of the proposed converter is based on the method proposed in [10]. Fig. 4 shows the carrier based modulation scheme for CUK-SSDTI. In this method, the offset values of upper and lower reference signals are defined as follows:

$$Offset_U = m_L \quad (1)$$

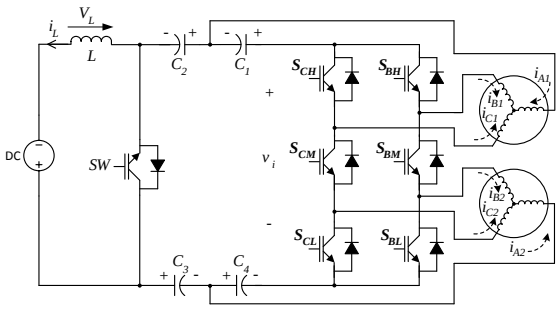


Fig. 3. The proposed buck-boost CUK-SSDTI

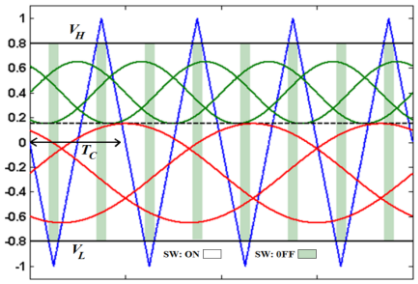


Fig. 4. The developed PWM scheme for CUK-SSDTI

$$Offset_L = -m_U \quad (2)$$

In Fig. 4, in addition to upper and lower reference signals, two extra reference signals V_H and V_L are used to control the conductive duty ratio of switch SW in boost circuit. Gate signal of SW switch is generated from comparing the V_H and V_L with the carrier signal. Using this method, the average volt-sec of the converter output voltages remain unchanged and also the minimum number of switching will be achieved.

$$\left(m_{U-\max} + m_{L-\max}\right) \le |V_H| + |V_L| \quad (3)$$

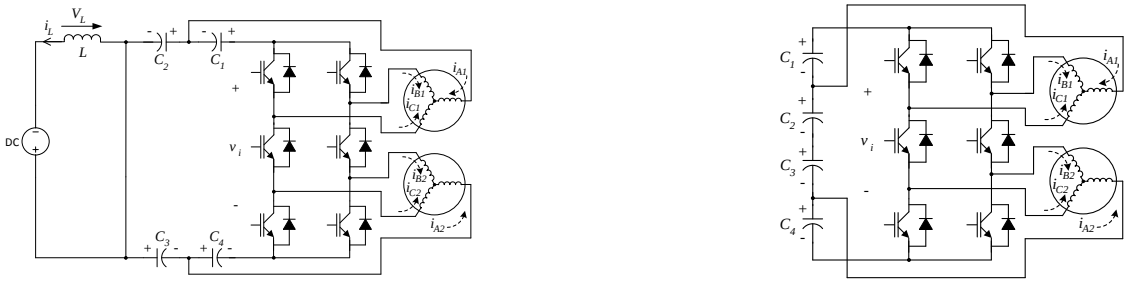
Choosing $|V_H|$=$|V_L|$=k, the time interval when switch SW is OFF will be symmetrical and the calculation of boost voltage gain and peak AC output voltage will be simplified. Fig. 5 shows the first operation mode of CUK-SSDTI when switch SW is off. In this mode, the inductor L is charged through SW and the capacitor voltage V_{C1}, the sum of the capacitor voltages V_{C2} and V_{C3}, and the capacitor voltage V_{C4} create, respectively, the upper, middle and lower DC source of SSDTI. Fig. 5(a) shows the equivalent circuit of CUK-SSDTI when SW is ON. The equivalent circuit of inverter side of the buck-boost converter is shown in Fig. 5(b). Considering Fig. 5, the following equation can be written.

$$V_L = V_{DC} \quad (4)$$

$$V_i = V_{C1} + V_{C2} + V_{C3} + V_{C4} = V_{C-Tot} \quad (5)$$

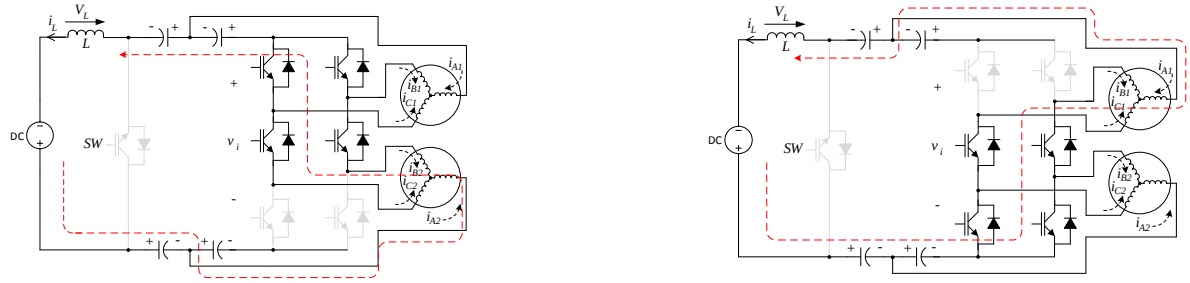
In second mode of operation (Fig. 6), switch SW is off and the inductor L is discharged through the shown paths and capacitors C_1 to C_4 will be charged with the voltage polarity specified on the figure. Fig. 6(a) shows the case that the carrier waveform is higher than reference signal V_H and Fig. 6(b) shows the case that the carrier waveform is lower than reference signal V_L. The inductor voltage in this mode is equal to

$$V_L = V_{DC} - V_{C-Tot} \quad (6)$$



(a) (b)

Fig. 5 Equivalent circuits of CUK-SSDTI in the first mode of operation (when SW is ON); (a) the overall equivalent circuit, (b) the inverter side equivalent circuit



(a) (b)

Fig. 6 Equivalent circuits of CUK-SSDTI in the second mode of operation (when SW is OFF); (a) the carrier waveform is higher than V_H, (b) the carrier waveform is lower than V_L.

Considering the fact that the average voltage of inductors over one switching period should be zero in steady state, the sum of capacitor voltages ($V_{C\text{-}Tot}$) is obtained as (7)

$$V_{C-Tot} = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \frac{V_{DC}}{1-k} \tag{7}$$

where k is duty cycle of switch SW in one switching period.

The effective input voltage of inverter (V_i) in first mode of operation (SW=ON) is defined as

$$v_i\big|_{SW:ON} = V_i = V_{C-Tot} = \frac{V_{DC}}{1-k} = B_{CUK} V_{DC} \tag{8}$$

B_{CUK} in above equation is called boost voltage gain of CUK converter and is equal to

$$B_{CUK} = \frac{1}{1-k} \tag{9}$$

As mentioned in [3], the DC-link capacitor voltages of SSDTI should be charged so that the outputs remain balanced and without offset. Following the same procedure for CUK-SSDTI and considering (7), it can be easily shown that the capacitor voltages can be expressed as (10) to (13).

$$V_{C1} = (1 - offset_U)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \tag{10}$$

$$V_{C2} = (offset_U - offset_L)\frac{V_{DC}}{4(1-k)} + \frac{V_{DC}}{2} \tag{11}$$

$$V_{C3} = (offset_U - offset_L)\frac{V_{DC}}{4(1-k)} + \frac{V_{DC}}{2} \tag{12}$$

$$V_{C4} = (1 + offset_L)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \tag{13}$$

Choosing the upper and lower offset according to (1) and (2), the capacitor voltages will be simplified as

$$V_{C1} = (1 - m_L)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \tag{14}$$

$$V_{C2} = (m_L + m_U)\frac{V_{DC}}{4(1-k)} + \frac{V_{DC}}{2} \tag{15}$$

$$V_{C3} = (m_L + m_U)\frac{V_{DC}}{4(1-k)} + \frac{V_{DC}}{2} \tag{16}$$

$$V_{C4} = (1 + m_U)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \tag{17}$$

It is possible to calculate the peak AC output voltages of the buck-boost inverter as

$$\hat{V}_{AC-U} = \frac{\sqrt{3}}{6}\frac{m_U V_{DC}}{(1-k)} \tag{18}$$

$$\hat{V}_{AC-L} = \frac{\sqrt{3}}{6}\frac{m_L V_{DC}}{(1-k)} \tag{19}$$

Clearly, the inverter AC outputs can be stepped up or down in relation to input DC voltage, by appropriate adjusting k, m_U and m_L. Although (18) and (19) infer that the CUK-SSDTI can theoretically achieve a high step-up voltage, in practice the step up voltage gain is generally limited due to the parasitic imperfections. Furthermore, adjusting large k is expected to affect the voltage stresses appearing across switches considerably since they are forced to turn OFF and ON within short time duration. To obtain a higher gain, while avoiding the use of a large k, the value of k could be optimally selected by

$$k = m_U + m_L \tag{20}$$

Therefore, in order to minimum voltage stress across switches, the peak AC output voltages of the buck-boost inverter are determined by

$$\hat{V}_{AC-U} = \frac{\sqrt{3}}{6}\frac{m_U V_{DC}}{(1-(m_U + m_L))} \tag{21}$$

$$\hat{V}_{AC-L} = \frac{\sqrt{3}}{6}\frac{m_L V_{DC}}{(1-(m_U + m_L))} \tag{22}$$

B. SEPIC-SSDTI Buck-Boost Converter

A SEPIC converter has same number of active and passive components as a CUK converter. However, this converter has advantage of having non-inverted output (the output has the same voltage polarity as the input). The input current in SEPIC converter is pulsating which is considered a disadvantage in running from a battery supply. The proposed SEPIC-SSDTI is shown in Fig. 7. This converter requires an extra active witch, an extra capacitor and an extra inductor compared with SSDTI.

The modulation technique applied to this converter is the same as shown in Fig. 4 and two reference signals V_H and V_L are employed to control switch SW. Again, to enhance DC bus utilization by increasing the maximum limit of modulation index, the upper and lower offset values are defined as (1) and (2) respectively. It should be noticed that the sum of upper and lower modulation indices should fulfill (3). When the carrier signal is lower than V_H and higher than V_L, switch SW is ON which is the first operation mode of the converter. In this case, as shown in Fig. 8, the inductor is charged by V_{DC} and the capacitor voltage V_{C1}, the sum of the capacitor voltages V_{C2} and V_{C3} as well as DC-link voltage V_{DC}, and the capacitor voltage V_{C4} create, respectively, the upper, middle and lower DC source of SSDTI. The second mode of operation (when SW is OFF) is shown in Fig. 9. Assuming $|V_H|=|V_L|=k$ and considering Figs. 8 and 9, and following the same method done for CUK-SSDTI, the important equations related to SEPIC-SSDTI can be derived which are tabulated in Table I.

According to Fig.8, the effective input voltage of inverter (V_i) in first mode of operation (SW=ON) is defined as

$$v_i\big|_{SW:ON} = V_i = V_{C-Tot} + V_{DC} = \frac{V_{DC}}{1-k} = B_{SEPIC}V_{DC} \quad (23)$$

As it is apparent in (23), the boost voltage gain of SEPIC-SSDTI (B_{SEPIC}) is similar to CUK-SSDTI. Also, capacitor voltages can be expressed as (24) to (27).

$$V_{C1} = (1-offset_U)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \quad (24)$$

$$V_{C2} = (offset_U - offset_L)\frac{V_{DC}}{4(1-k)} \quad (25)$$

$$V_{C3} = (offset_U - offset_L)\frac{V_{DC}}{4(1-k)} \quad (26)$$

$$V_{C4} = (1+offset_L)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \quad (27)$$

Choosing the upper and lower offset according to (1) and (2), the capacitor voltages will be simplified as

$$V_{C1} = (1-m_L)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \quad (28)$$

$$V_{C2} = (m_L + m_U)\frac{V_{DC}}{4(1-k)} \quad (29)$$

$$V_{C3} = (m_L + m_U)\frac{V_{DC}}{4(1-k)} \quad (30)$$

$$V_{C4} = (1+m_U)\frac{V_{DC}}{2(1-k)} - \frac{V_{DC}}{2} \quad (31)$$

The peak AC output voltages of SEPIC-SSDTI are similar to CUK-SSDTI as shown in Table I. Based on the proposed method for minimizing the switch voltage stresses, the value of k is again determined by (20) and thus the peak AC output voltages of SEPIC-SSDTI are similar to (18) and (19).

C. Diode-Assisted SSDTI Buck-Boost Converter

The proposed Diode-Assisted SSDTI is composed of SSDTI and an X-shaped diode–capacitor network. Fig. 10 shows the proposed topology of this converter. Diode-Assisted SSDTI has two extra diodes compared with CUK and SEPIC-SSDTI. The same modulation technique as shown in Fig. 4 is

TABLE I. RELATIONS OF PROPOSED BUCK-BOOST CONVERTERS BASED ON SSDTI

	CUK-SSDTI	SEPIC-SSDTI	Diode-Assisted SSDTI
$V_{C\text{-}Tot}$	$\frac{V_{DC}}{1-k}$	$\frac{kV_{DC}}{1-k}$	$\frac{2V_{DC}}{1-k}$
$v_i\|_{SW=ON} = V_i$	$\frac{V_{DC}}{1-k}$	$\frac{V_{DC}}{1-k}$	$\frac{2V_{DC}}{1-k}$
B	$\frac{1}{1-k}$	$\frac{1}{1-k}$	$\frac{2}{1-k}$
$\hat{V}_{AC-x}$	$\frac{\sqrt{3}}{6}\frac{m_x V_{DC}}{(1-k)}$	$\frac{\sqrt{3}}{6}\frac{m_x V_{DC}}{(1-k)}$	$\frac{\sqrt{3}}{3}\frac{m_x V_{DC}}{(1-k)}$

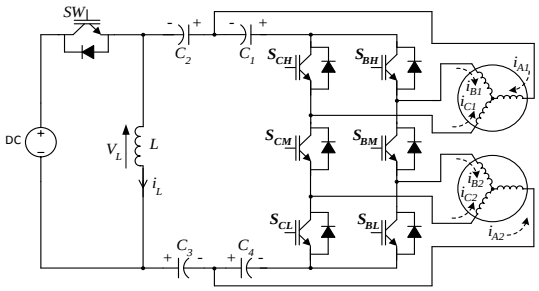
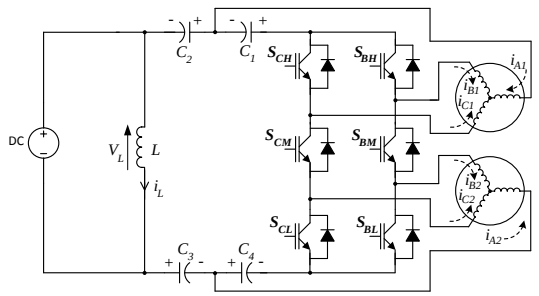
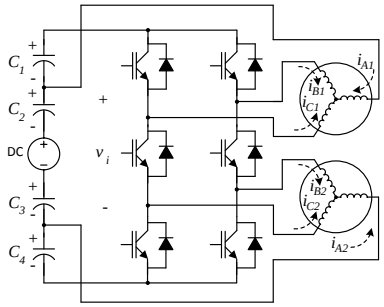


Fig. 7. The proposed buck-boost SEPIC-SSDTI

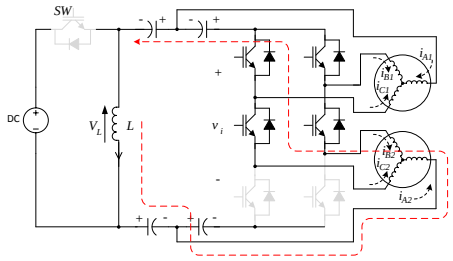


(a)

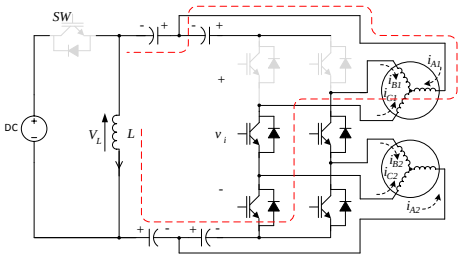


(b)

Fig. 8 Equivalent circuits of SEPIC-SSDTI in the first mode of operation (when SW is ON); (a) the overall equivalent circuit, (b) the inverter side equivalent circuit



(a)



(b)

Fig. 9 Equivalent circuits of SEPIC-SSDTI in the second mode of operation (when SW is OFF); (a) the carrier waveform is higher than V_H, (b) the carrier waveform is lower than V_L.

used for Diode-Assisted SSDTI in order to be able to fairly compare it with two other proposed buck-boost converters. Figs. 11 and 12 show two operation modes of Diode-Assisted SSDTI and the related equations are tabulated in Table I. The inductor voltage and input voltage of SSDTI in second operation mode are equal to

$$V_L = V_{DC} - (V_{C1} + V_{C2}) = V_{DC} - (V_{C3} + V_{C4}) = V_{DC} - \frac{V_{C-Tot}}{2} \tag{32}$$

$$V_i = V_{C1} + V_{C2} = V_{C3} + V_{C4} = \frac{V_{C-Tot}}{2} \tag{33}$$

The important equations related to Diode-Assisted SSDTI are tabulated in Table I. According to Fig.11, the effective input voltage of inverter (V_i) in first mode of operation (SW=ON) is defined as

$$v_i\big|_{SW:OFF} = V_i = V_{C-Tot} = \frac{2V_{DC}}{1-k} = B_{Diode-A} V_{DC} \tag{34}$$

As it is apparent in (43), the boost voltage gain of Diode-Assisted SSDTI ($B_{Diode\text{-}A}$) is twice of B_{CUK} and B_{SEPIC}. Also, capacitor voltages can be expressed as (10) to (13).

$$V_{C1} = (1 - offset_U)\frac{V_{DC}}{(1-k)} - \frac{V_{DC}}{2} \tag{35}$$

$$V_{C2} = offset_U \frac{V_{DC}}{2(1-k)} + \frac{V_{DC}}{2} \tag{36}$$

$$V_{C3} = -offset_L \frac{V_{DC}}{2(1-k)} + \frac{V_{DC}}{2} \tag{37}$$

$$V_{C4} = (1 + offset_L)\frac{V_{DC}}{(1-k)} - \frac{V_{DC}}{2} \tag{38}$$

Choosing the upper and lower offset according to (1) and (2), the capacitor voltages will be simplified as

$$V_{C1} = (1 - m_L)\frac{V_{DC}}{(1-k)} - \frac{V_{DC}}{2} \tag{39}$$

$$V_{C2} = m_L \frac{V_{DC}}{2(1-k)} + \frac{V_{DC}}{2} \tag{40}$$

$$V_{C3} = m_U \frac{V_{DC}}{2(1-k)} + \frac{V_{DC}}{2} \tag{41}$$

$$V_{C4} = (1 + m_U)\frac{V_{DC}}{(1-k)} - \frac{V_{DC}}{2} \tag{42}$$

It is possible to calculate the peak AC output voltages of the buck-boost inverter as

$$\hat{V}_{AC-U} = \frac{\sqrt{3}}{3}\frac{m_U V_{DC}}{(1-k)} \tag{43}$$

$$\hat{V}_{AC-L} = \frac{\sqrt{3}}{3}\frac{m_L V_{DC}}{(1-k)} \tag{44}$$

To minimum voltage stress across switches, the value of k is again determined by (20) and thus the peak AC output voltages of the buck-boost inverter are expressed as

$$\hat{V}_{AC-U} = \frac{\sqrt{3}}{3}\frac{m_U V_{DC}}{(1-(m_U + m_L))} \tag{45}$$

$$\hat{V}_{AC-L} = \frac{\sqrt{3}}{3}\frac{m_L V_{DC}}{(1-(m_U + m_L))} \tag{46}$$

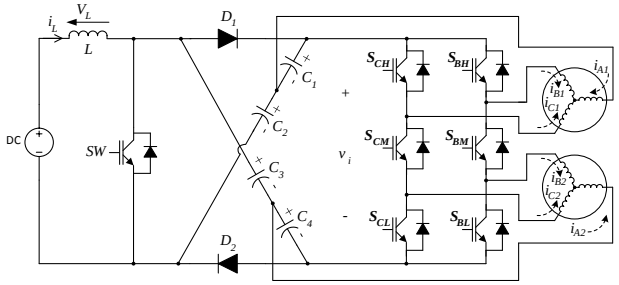
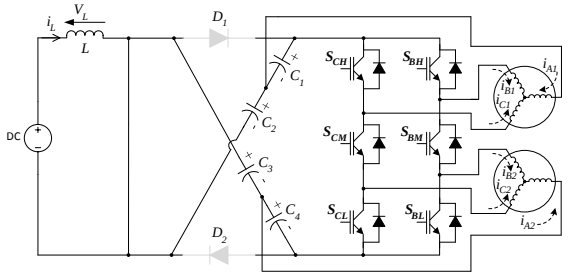
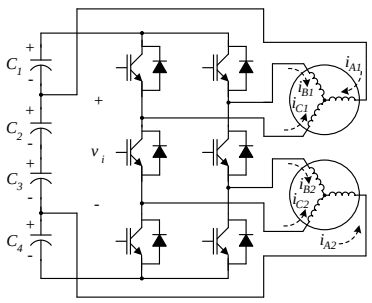


Fig. 10. The proposed buck-boost Diode-Assisted SSDTI

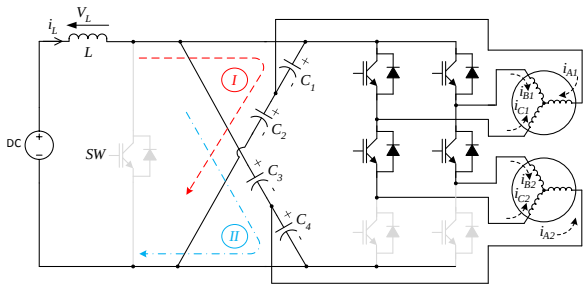


(a)

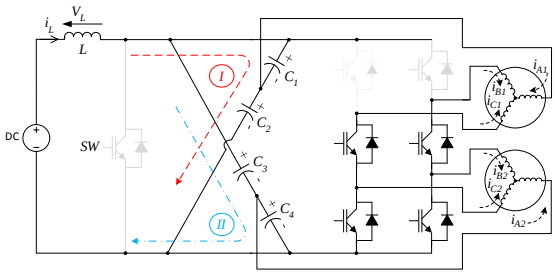


(b)

Fig. 11 Equivalent circuits of Diode-Assisted SSDTI in the first mode of operation (when SW is ON); (a) the overall equivalent circuit, (b) the inverter side equivalent circuit



(a)



(b)

Fig. 12 Equivalent circuits of Diode-Assisted SSDTI in the second mode of operation (when SW is OFF); (a) the carrier waveform is higher than V_H, (b) the carrier waveform is lower than V_L.

IV. Simulation and Experimental Results

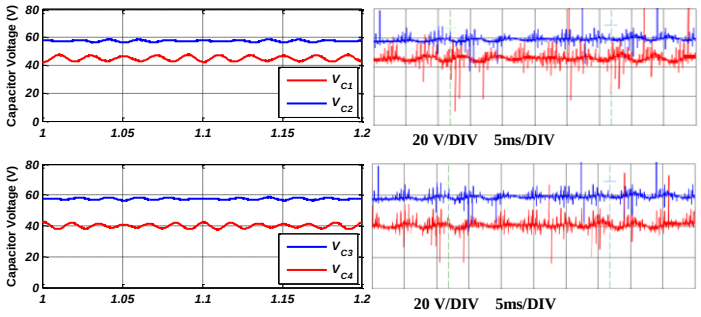
In this section, the performance and the validity of the proposed buck-boost converters are investigated by simulation and experimental results. Two resistive-inductive loads are connected to the outputs of SSDTI. The control scheme has been implemented on a TMS320F2812 DSP. Simulation and experimental parameters are listed in Table II. The DC bus voltage level is chosen for the three converters so that the amplitude of the output current is the same. The input DC voltage of CUK-SSDTI and SEPIC-SSDTI are equal to 40 V, while the input DC voltage of Diode-Assisted SSDTI is 20V.

Fig. 13 shows simulation and experimental waveforms of the capacitor voltages of CUK-SSDTI. It is worth noticing that capacitor voltages have abided by equations previously obtained in (10) to (13) and their values are equal to 45, 57.5, 57.5 and 40 V respectively. Fig. 14 shows the DC bus voltage of CUK-SSDTI that alters between the expected values. Figs. 15 and 16 show upper and lower terminals waveforms of CUK-SSDTI, respectively. As is reflected in these figures, the frequency and amplitude of the waveforms are at the expected values and the current waveforms are balanced without DC component.

Fig. 17 shows simulation and experimental waveforms of the capacitor voltages of SEPIC-SSDTI. Again, the DC-link

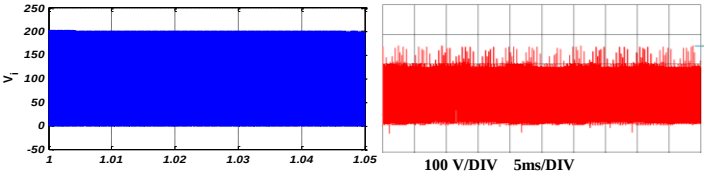
TABLE II. Simulation and Experimental Results

Parameter	Value	Parameter	Value
Switching Frequency	10 kHz	R_{load}	25 Ohm
f_U	50 Hz	L_{load}	25 mH
f_L	60 Hz	L	15 mH
m_U	0.4	C_1 & C_2& C_3& C_4	1000 uF
m_L	0.35	V_{DC} *(CUK and SEPIC)*	40 V
B_{CUK}	5	V_{DC} *(Diode Assisted)*	20 V
B_{SEPIC}	5	k	0.8
$B_{Diode\text{-}A}$	10		



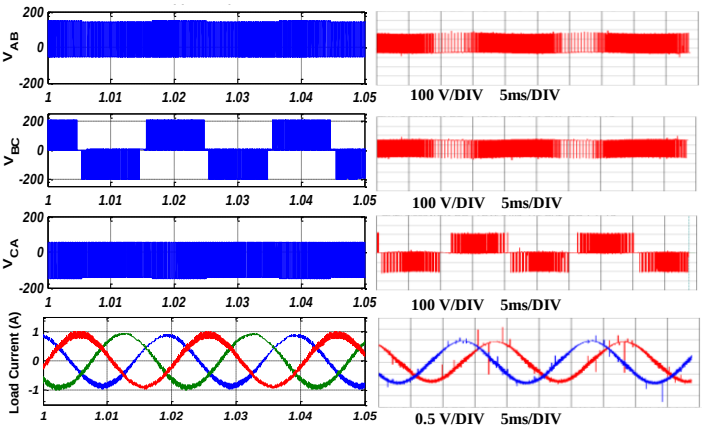
(a) (b)

Fig. 13. DC link capacitor voltages of CUK-SSDTI , (a) Simulation results, (b) Experimental results



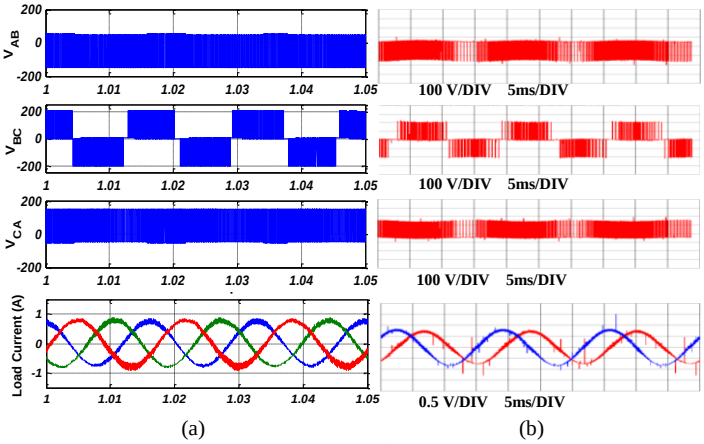
(a) (b)

Fig. 14.DC bus voltage (V_i) of CUK-SSDTI , (a) Simulation results, (b) Experimental results



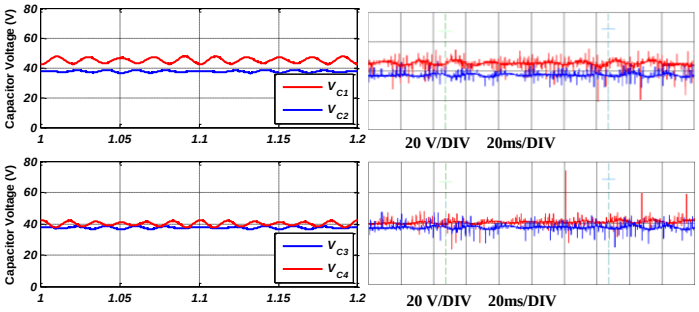
(a) (b)

Fig. 15. CUK-SSDTI upper terminal waveforms, (a) Simulation results, (b) Experimental results



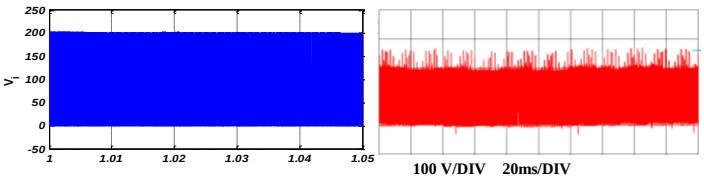
(a) (b)

Fig. 16. CUK-SSDTI lower terminal waveforms, (a) Simulation results, (b) Experimental results



(a) (b)

Fig. 17. DC link capacitor voltages of SEPIC-SSDTI , (a) Simulation results, (b) Experimental results



(a) (b)

Fig. 18.DC bus voltage (V_i) of SEPIC-SSDTI , (a) Simulation results, (b) Experimental results

capacitors are automatically charged at the expected voltage levels based on equations (24) to (27) which are equal to 45, 37.5, 37.5 and 40 V respectively. In this case the upper and lower output waveforms resemble Figs. 15 and 16 and are not depicted. Fig. 18 shows the DC bus voltage of SEPIC-SSDTI. As it was expected V_i in this case changes between 0 and 200V. Fig. 19 shows simulation and experimental waveforms of the capacitor voltages of Diode-Assisted SSDTI which has settled at the anticipated levels of 55, 45, 50 and 50 V in accordance with (35) to (38). The upper and lower output waveforms in Diode-Assisted SSDTI are again similar to Figs. 15 and 16. Also, Fig. 20 shows the DC bus voltage of Diode-Assisted SSDTI which alters between 100V and 200V.

V. CONCLUSION

In this paper three new buck-boost inverters based on SSDTI were proposed with two three-phase AC outputs and one DC input. The proposed buck-boost inverters are CUK-SSDTI, SEPIC-SSDTI and Diode-Assisted SSDTI. In addition to boosting the voltage, these converters require minimum number of active switches compared with counterpart topologies. Therefore the proposed converters can lead to reduction in necessary associated hardware, markedly gate drive and protection circuits, and cooling system, which, in turn, have a considerable impact on system volume, weight and cost. The boost voltage gain of CUK-SSDTI and SEPIC-SSDTI are similar, whereas the boost voltage gain of Diode-Assisted SSDTI is twice. Simulation and experimental results verified performance and validity of the proposed converters.

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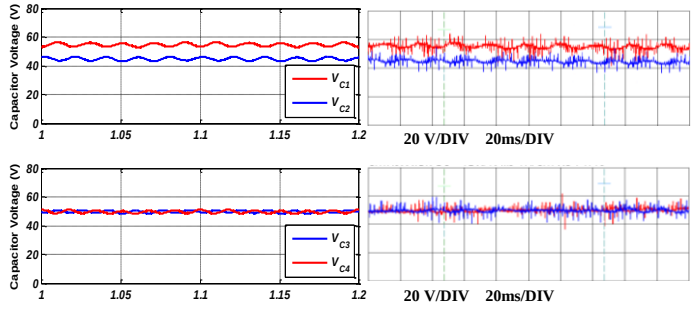
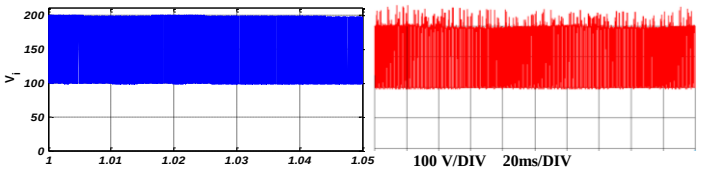


(a) (b)

Fig. 19. DC link capacitor voltages of Diode-Assisted SSDTI , (a) Simulation results, (b) Experimental results



(a) (b)

Fig. 20 .DC bus voltage (V_i) of Diode-Assisted SSDTI , (a) Simulation results, (b) Experimental results

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