

A Differential Dual delay mode Schmitt Trigger with 449ps delay gap by Reconfiguring with one bit and FVF current source

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Abstract—In this paper a new dual delay mode Schmitt Trigger (ST) with adjustable delay and hysteresis width in run time and design time is proposed. This delay element, can reconfigure by a digital mode select bit from ST mode to comparator mode and the input to output delay changes 449ps (7.97GHz frequency shift). Also it has tunable delay by changing bias of the feedback Flipped Voltage Follower (FVF) current source in design time. The proposed differential Schmitt trigger has SCL based design which keeps the power profile almost uniform vs changing the delay. Differential configuration make a low delay variation in Monte Carlo analysis 0.129ppm (234.4mv deviations in 1800mv) in hysteresis. The power consumption and delay of proposed delay element are 103-581ps and 4.23-1.04mW for ST and comparator mode, sequentially. The simulations results are in CMOS 180nm standard technology. The conclusion is that the dual band Schmitt trigger is appropriate in multi band and high performance applications.

Keywords—Schmitt trigger (ST); Adjustable; Hysteresis; Run time; Design time; Reconfigure; Flipped Voltage Follower (FVF).

I. INTRODUCTION

Schmitt trigger is a positive feedback/ feed forward element which is used in many applications such as SRAM's based on Schmitt trigger circuit [1]. This ST cell has better read/write stability rather than other SRAMs, Masking soft errors of latches of logic systems and memories in VLSI circuits by ST [2], ST based latch design for overcoming soft errors [3], edge detection of finger prints [4], lowering on-to-off leakage current at output node of gates using Schmitt trigger [5], class D amplifiers as comparator [6]. Schmitt trigger has the property of reduction of signal transition so the static power consumption will reduce. Also in delay cell applications such as Digital Controlled Oscillator (DCO) for power optimization, delay shift and input noise elimination [7, 8]. First CMOS well-known Schmitt trigger is belong to [9]. Its ST has 4 transistor stack and creates a current path between VDD and GND. So it is not desirable in ultra-low power/voltage applications. Also it is single ended with fixed hysteresis width set by device domination. Other ST by inspiration from [9] are presented to reduce power and voltage or improve PVT stabilization [10,

11]. In [10] the power and voltage reduces by inserting two transistor as footer and header to control current. The signal from second transistor feedback has weak logic so it is sensitive to PVT changes. [11] is a Schmitt trigger delay cell with incremental structure for bigger delay but with same power consumption. It has no current path from VDD to GND and is more PVT tolerant because of strong logic level in every points of circuits. It will become more complex and occupy large area for bigger delay in design time. RS Schmitt trigger [12] with better temperature response is single ended with fixed hysteresis and has more transistor than conventional ST. [13, 14] are two and one side tunable hysteresis width in design time, sequentially. Bulk driven ST is used in [7, 15]. It is a reconfigurable single end ST by a digital mode bit and utilizes two delay in run time but the delay is fixed, set by device dimension. [16] differential input single output adjustable hysteresis (delay) Schmitt trigger is a current regenerative type which its delay adjustment is in design time by bias and sizing. This differential St can use in differential circuit by an intermediate device (single end to differential ended converter). In this paper we proposed a new dual band fully differential Schmitt trigger based on SCL inverters and positive feedback to have two different delay band in run time and adjustable delay set by feedback FVF current source. Also each SCL inverter has a current tail that can vary the delay. SCL comparator used is cross coupled which ensures full swing without use of replica bias circuit [17] in cascading and provides the noise margin of next stage. The SCAL nature of proposed circuit make Power delay product (PDP) almost independent from frequency increment. This make this ST suitable for high-performance low-power applications. The paper organization is as follow: The circuit are described in Section 2. Compare and review of proposed circuits and conventional STs with simulation results are discussed in Section 3. Finally, Section 4 concludes this paper.

II. CIRCUIT DESCRIPTION

A. Circuit topology

Schmitt trigger has a positive feedback to generate a hysteresis in in-out characteristic. Figure 1, shows the procedure to final idea of proposed fully differential Schmitt trigger. Main idea of reconfigurable differential Schmitt trigger is illustrated in Figure 1 (a). It consists of two SCL cross coupled comparator SCL inv 1, 2 with $I_{ss_inv1, 2}$.

A differential symmetric feedback from output to intermediate between comparators. The feedback has two bias VN, VP. These bias set the hysteresis width in design time. Two multiplexer each one consist of two transistor are act as delay

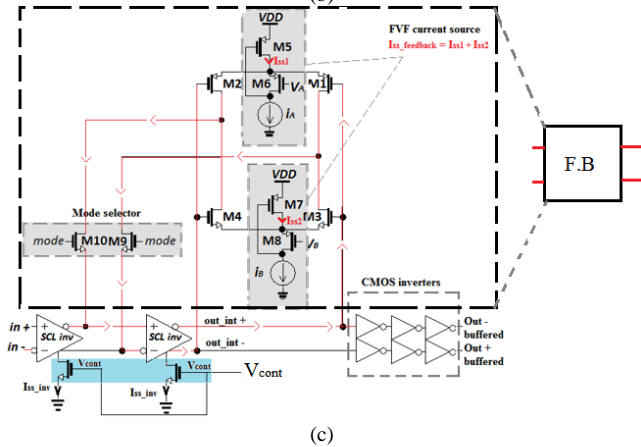
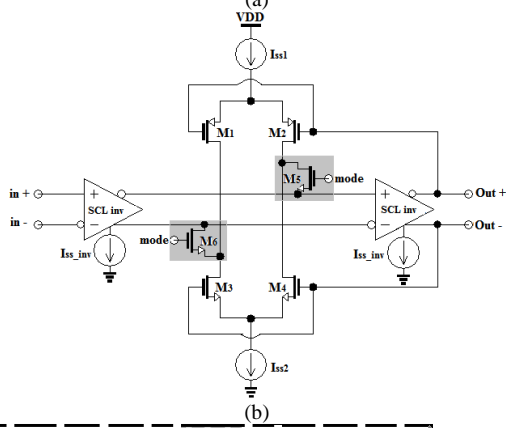
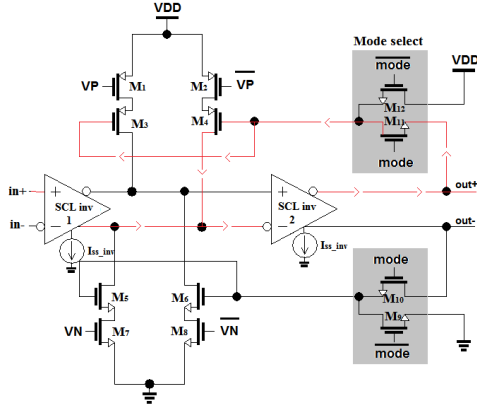


Figure 1. Proposed differential dual delay mode Schmitt trigger. (a) Main idea. (b) Modified Schmitt trigger. (c) Final modified proposed Schmitt trigger.

When mode bit is high, the feedback is connected and otherwise it is omitted. Figure 1 (b) is simplified model of Figure 1 (a). The bias transistors $M_{1, 2, 7, 8}$ are replaced by two current source $I_{ss1, 2}$. Each MUX changes to a single transistor as a switch, which by mode instruction connects the separate feedback to the intermediate nodes of comparator connection.

Final circuit of differential dual delay mode Schmitt trigger is shown in Figure 1 (c). The hysteresis width control current sources are replaced with FVF current source. It is because of wider range of current variations. Therefore, the range of hysteresis and delay changes increase. The $I_{ss_inv1, 2}$ are two NMOS transistor which their gates are control by V_{cont} bias. The CMOS buffer chain added at the end of SCL based Schmitt trigger to have mode sharper pulses.

The SCL comparators used in feedforward path and the SCL block of feedback has delay which is follows from (1).

$$\tau_{SCL} = R_L \cdot C_L \approx V_{sw} / I_{ss} \cdot C_L \quad (1)$$

Where R_L is equivalent PMOS load resistance, C_L is overall output capacitance, V_{sw} is swing of output signals and I_{ss} is SCL current tail. The delay is proportional to load capacitance, voltage swing, and inversely to current tail of I_{ss} . In the proposed design, the output transistors, the capacitance load and the delay, will change by reconfiguring the structure from ST to comparator-mode. VTC curve of proposed ST in hysteresis ST mode with low delay.

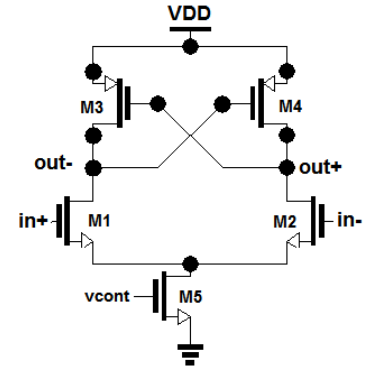


Figure 2. Cross coupled SCL comparator.

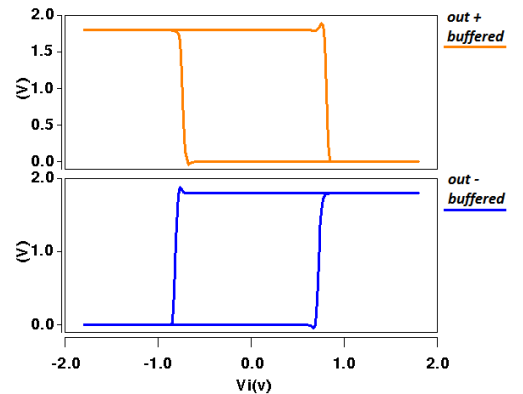


Figure 3. Hysteresis characteristic of proposed differential Schmitt trigger in ST mode, @ $V_{bias} = 1.6v$ and $V_{cont} = 0.9v$.

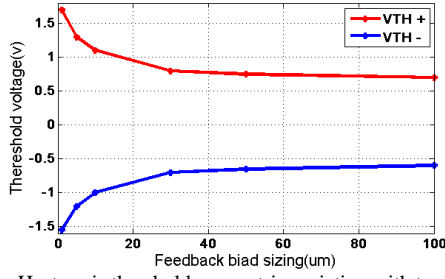


Figure 4. Hysteresis threshold symmetric variation with tuning the FVF current source by transistor sizing $M_{6,8}$ in design time.

B. Comparison

To have better comparison of proposed we modified conventional Schmitt trigger shown in Figure 5. It has mode select switches and MUX for feedback elimination to have dual band delay. It has a replica with reverse input to have full differential output and CMOS buffer for pulse sharpening. By comparing the proposed dual mode delay element and conventional the curve of delay and power delay product (PDP) are extracted, Figure 6 (a, b). Figure 6 (a) shows that delay of SCL mode is independent of feedback bias variations because feedback eliminates in SCL comparator mode. Therefore, by adding up the feedback and increment of I_{ss} according to (1), delay of SCL mode is more than ST mode. In conventional ST delay vs I_{ss} is more similar to SCL logic. And opposite of proposed ST, delay of ST mode is more due to bigger C_L . Figure 6 (b), shows more power consumption for conventional ST because of more complex structure and also current path between VDD and GND. But ST mode in both design consumes more power because of feedback. Feedback creates more current paths for power consumptions. In proposed Schmitt trigger, $I_{ss1,2}$ for comparator are the main power consumption reasons and $I_{ss_feedback}$ is almost negligible against them. So power variation vs $I_{ss_feedback}$ changes is almost independent. This means delay variations implies a little power increment.

Figure 7 (a, b) presents, radar diagram comparison of designs with conventional. The chart is normalized to ST mode in conventional design. The most power and PDP belong to convention design ST mode because it's more complexity and current path between VDD/GND. But proposed design has more and less delay. Therefore the delay gap between this two modes is higher in our design which utilizes a high frequency gap. Also our design consumes less power than a circuit with similar characteristics (conventional design) because of SCL nature of it. Overall evaluation and review of Schmitt triggers is summarized in TABLE I. it shows proper performance of this proposed dual band delay Schmitt trigger.

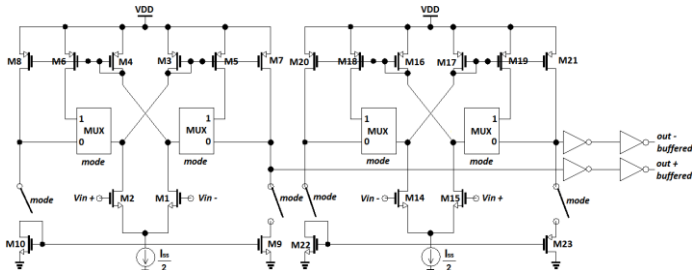


Figure 5. Modified conventional Schmitt trigger.

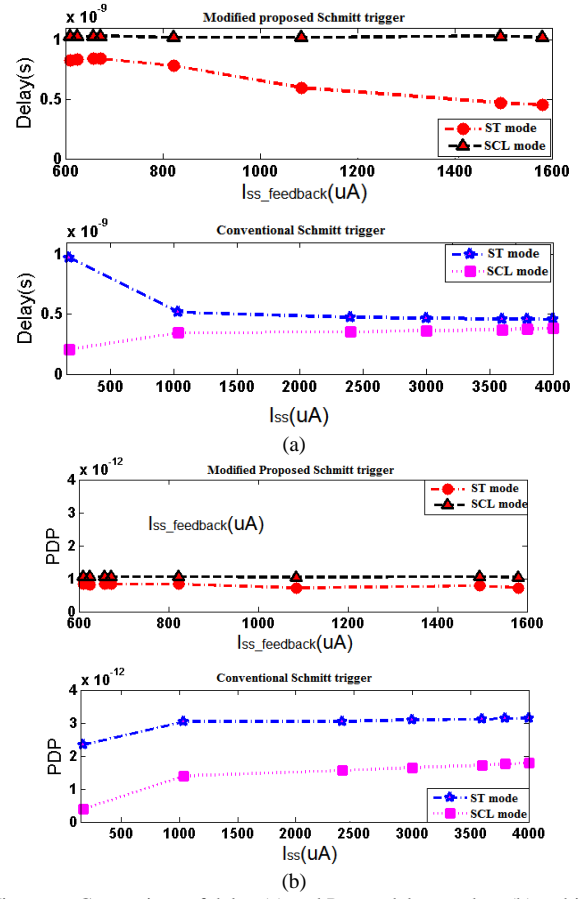


Figure 6. Comparison of delay (a) and Power delay product (b) vs bias variation of proposed and conventional Schmitt trigger.

■ Comparator mode ■ ST mode

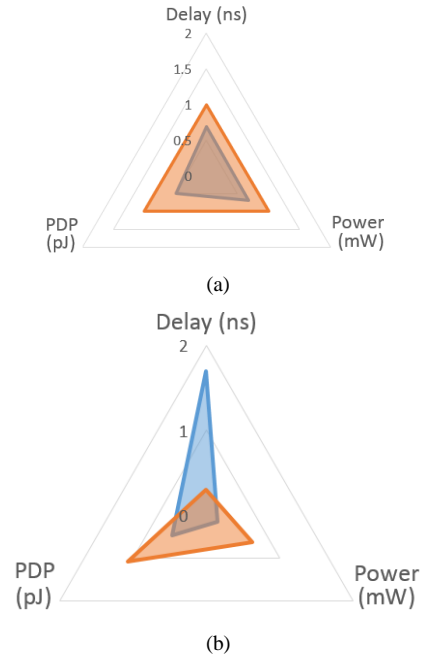


Figure 7. Radar chart compare of conventional (a) Schmitt trigger @ $V_{bias}=1.6v$ and proposed (b) $V_{bias}=1.6v$.

TABLE I. EVALUATION AND COMPARISON OF PROPOSED SCHMITT TRIGGER

* S: Single / D: Differential

	[9]	[10]	[16]	[11]	[7]	Conventional ST		proposed ST	
						SCL Mode	ST Mode	SCL Mode	ST Mode
Input architecture	S*	S	D*	S	S	D		D	
Output architecture	S	S	S	S	S	D		D	
Supply voltage (v)	5	3	1.8	1	1.8	1.8		1.8	
L min (nm)	-	120	180	90	180	180		180	
Swing voltage (v)	5	3	1.8	-	1.8	1.8		1.8	
Number of transistor	6	6	14	12	8	26	32	12	20
Variable hysteresis	NO	Yes	Yes	NO	NO	Yes		Yes	
Reconfigurable structure	NO	NO	NO	Yes	Yes	Yes		Yes	
Delay change time	-	Design time	Design time	Design time	Run time	Design/Run time		Design/Run time	
Delay change mechanism	-	-	Transistor Sizing / Bias	Structure change	Digital code	Digital code/ Bias/Sizing		Digital code/ Bias/Sizing	
I _{ss} bias Implementation	-	-	Single NMOS	-	-	Single NMOS		FVF	
Power consumption	High	Low	Mid.	Low	Mid.	High		Mid.	
Power Delay Product (p. J)	-	-	-	342e6	-	1.12	2.28	1.07	2.45
Delay Step (ps)	-	-	Not report	170	3.495	94 @ 1.4v bias (247~ 341ps)		449 @ 1.6v bias (103~581ps)	

Small signal model of proposed design can give us an estimation of delay in theory. Using half circuit of Figure 1 (c) and symmetric and neglecting transistor switches because of their negligible effect on delay the simplified small signal model of circuit is illustrates in Figure 8.

$$\begin{aligned}
 C_1 &= C_{gb2} + C_{gs2} & C_{out} &= C_{db7} \\
 g_{mi} &= g_{m2} & R_{mid} &= r_{o2} || r_{o8} || 1/g_{m3} \\
 g_{mii} &= g_{m7} & V_x & \text{ is drain voltage of } M_2 \\
 C_f &= C_{gd7}
 \end{aligned} \quad (2)$$

Transfer function of circuit Figure 8 is shown in (3).

$$H(s) = \frac{-(C_{out}R_{out}s + 1)(g_{m7} - C_{fs})(g_{m1} - C_{gd1}s)(g_{m7} - C_{fs} + C_{mid}s + C_{mid}g_{m7}R_{in}s - C_f C_{mid}R_{in}s^2)}{s(C_{mid}R_{in}s + 1)(C_f + C_{out} + C_f C_{out}R_{out}s)} \quad (3)$$

Using of ailoto [18] method for delay approximate equation. We use the pole of function (3). The dominant pole which determines the delay approximately. By replacing natural frequency s with $j2\pi f$, the propagation delay of delay element is inversely proportion to dominant pole of (3) as shown in (4).

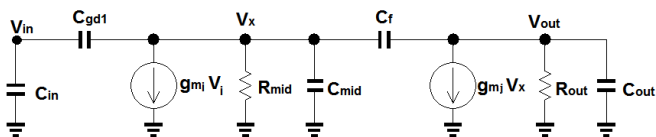


Figure 8. Small signal model of proposed Schmitt trigger in ST mode.

$C_{dbf2} + C_{dbf4}$ are the elements from feedback which eliminates in lower band frequencies. Therefore, the band1 delay equation is as (4). Comparison of (4, 5) shows that frequency at lower delay band (SCL comparator mode) would be higher than upper delay band (ST mode) due to feedback.

$$\tau_{p,lower \text{ delay band}} = \frac{C_{mid}R_{in}}{2\pi} \approx \quad (4)$$

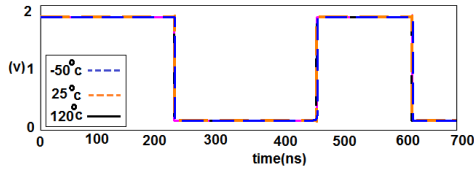
$$\tau_{p,upper \text{ delay band}} = \frac{C_{mid}R_{in}}{2\pi} \approx \frac{(C_{gb5} + C_{gs5} + C_{db3} + C_{db1} + C_{dbf2} + C_{dbf4}) \left(-\frac{1}{g_{m3}} \right)}{2\pi} \quad (5)$$

Simulation and analytical calculations are showing same results and agrees.

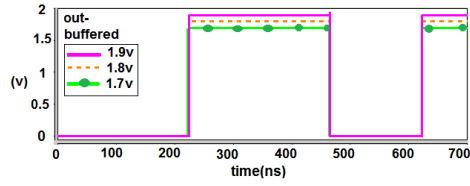
III. SIMULATION AND RESULTS

The PVT tests are shown in Figure 9 (a, b) and Figure 10 (a, b and c), sequentially. The analysis shows circuit validity.

Fully differential Schmitt-trigger with customizable structure by a digital bit is introduced and simulated in 0.18 μ m. the power, delay and hysteresis different from one structure to another in run time. This design creates a delay gap of 244ps and is a low power hysteresis mutable delay cell.

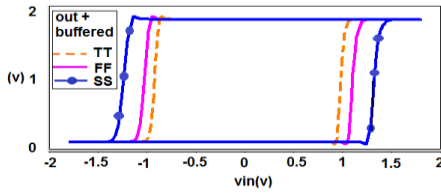


(a)

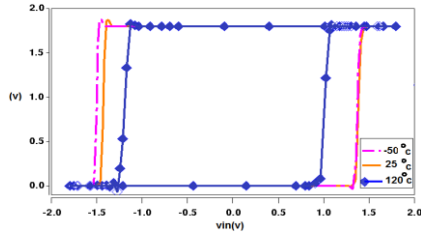


(b)

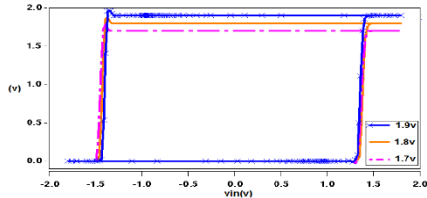
Figure 9. Temperature (a) and supply voltage (b) analysis effect on output signal.



(a)



(b)



(c)

Figure 10. Corner (a), temperature (b) and supply voltage (c) analysis effect on hysteresis thresholds deviation.

Suitable in multi frequency band applications (i.e. Digital Controlled Oscillator). In addition each operational mode of proposed circuits has tunable hysteresis width and delay which tunes in design time by bias or sizing or current steering value. Conventional circuit with lower delay (247~341ps) consumes more power (4.57~6.71mW) and its frequency step is less (94ps creates 1.1GHz frequency gap between bands, N is number of cascade stages) than proposed design (delay 103~581ps, power 1.04~4.23mW, delay step 449ns and frequency gap 7.97GHz). Hysteresis threshold deviation in Monte Carlo analysis for proposed Schmitt-trigger is 232.5mv

per 1800mv (0.129ppm).The simulation results shows operation validity of the proposed design.

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