A novel high swing, low power Charge Pump circuit with excellent current matching

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Abstract— **A new charge pump (CP) circuit is proposed in this paper. This circuit utilizes a gain boosting technique to achieve a high output impedance over a wide output voltage range. By using a simple gain boosting circuit, good current matching characteristics can be achieved with less than 0.25µA, less than 0.5%, difference of the UP/DN current over CP output voltage range. A high output voltage swing is obtained by employing the bulk driven technique. The proposed CP circuit is designed and simulated under 1.8V power supply in 0.18µm CMOS technology in HSPICE.**

Keywords- charge pump; bulk driven; gain boosting; current mirror.

I. INTRODUCTION

The charge pump phase locked loops (CPPLLs) are generally used in modern communication systems with a high frequency clock signal. The CPPLL consists of a phase/frequency detector (PFD), charge pump (CP), a loop filter (LF) and voltage controlled oscillator (VCO). A typical CPPLL system is shown in Fig 1.

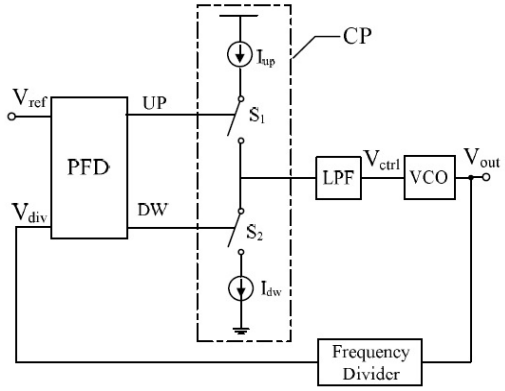


Figure 1. A charge pump phase locked loop (CPPLL)

The main function of CP is to convert the duration of the UP and DN signals, generated by PFD, into an accurate amount of charge that delivered to or extracted from LPF [3]. Therefore, the performance of the PLL loop will be decreased by non-idealities of the charge pump circuit. A well-designed charge pump circuit must has an excellent current matching characteristic, up to 98%, to reduce the value of phase offset. In addition, to reduce the value of the loop bandwidth variation, the variation of the output current amplitude due to the change of the output voltage must be minimized.

Authors in [1] proposed a charge pump with gain-boosting technique. The output resistance is increased. But, the output voltage swing is low and its power consumption is high. In [2], a bulk driven cascode current mirror is used to increase the output resistance. However, the output resistance is not high enough. In [3] a rail-to-rail operational amplifier is used to enable the charge and discharge currents to be matched well in a wide output voltage range. In [4] an adaptive body bias charge pump circuit is introduced. The circuit uses a number of resistances to compensate current variations. However, the value of these resistances will be changed by multiple parameters such as temperature and fabrication, and are not reliable.

In this work, a new CP circuit is designed. This circuit uses a gain boosting technique to increase the output resistance of a CP. Therefore, a good current matching characteristic is achieved. Furthermore, using the bulk-driven technique increases the outputs swing and decreases the value of the threshold voltage and the power consumption.

II. GAIN BOOSTING

A conventional CMOS CP circuit usually has UP and DN switches made of pMOS and nMOS transistors, respectively. The current mismatch, between Up and Down paths, strongly depends on the output impedances of pMOS and nMOS path switches as dumping or sinking the charge to or from LPF. In this section a new CP circuit is proposed, using gain boosting technique, to increase the output impedance of the charge pump circuit.

The gain boosting method, which is applied to increase the output impedance, is indicated in Fig.2 [1]. The idea is to drive the gate of M2 by an amplifier that forces Vx to be equal to Vb. Therefore, Due to the smaller variations at node x, the current through ro1 and hence the output current will remain more constant.

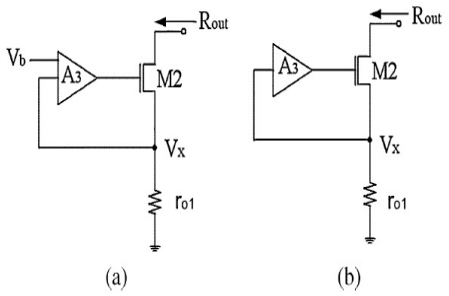


Figure 2. (a) Concept of the gain-boosting circuit. (b) Simplified gain-boosting circuit.

It means that, a high output impedance is achieved using the gain boosting method. The output resistance of the gain boosting circuit (Fig.2) is given as follows:

Rout =A3 gm2 ro2 ro1 (1)

It is observed that, Rout is boosted significantly without the need to stack more cascode devices on top of M2. Vb can be set to zero for small-signal operation. Therefore the circuit of Fig.2(b) is achieved.

The circuit can be implemented, using the single transistor amplifier (M3) which is shown in Fig. 3. The output resistance of this circuit, which is similar to the output resistance of a triple-cascode circuit, is obtained as follow:

Rout = (gm2ro2ro1)(gm3ro3). (2)

Trying the above idea, a new CP circuit is designed which is depicted in Fig. 4.

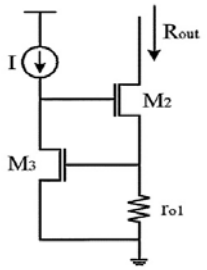


Figure 3. Gain-boosting circuit

Fig. 4 indicates the proposed CP circuit. Ibias1 and Ibias2 are current sources for the single-transistor amplifiers of M9 and M14. The output resistance of M10 and M11 can be modeled as ro1, in Fig.3. When the DN signal is active, M12 and M14 will operate, in conjunction with M11, to provide a gain boosting circuit. The output resistance of the UP and DN paths are obtained as follows,

$$R_{out,dn} = [gm_{12}ro_{12}(gm_{11}ro_{13}ro_{11})](gm_{14}ro_{14}) \quad (3)$$

$$R_{out,up} = [gm_{7}ro_{7}(gm_{10}ro_{8}ro_{10})](gm_{9}ro_{9}) \quad (4)$$

To increase the current matching and output impedance of UP and DN paths, the aspect ratios of transistors are adjusted to obtain Rout,dn= Rout,up. By increasing the output resistance of the CP circuit, an excellent current matching characteristic is obtained. The gain boosting CP is suitable for low power supply voltage because it does not require stacking more cascode devices to increase the output resistance. The output voltage swing is increased further by using a bulk driven technique.

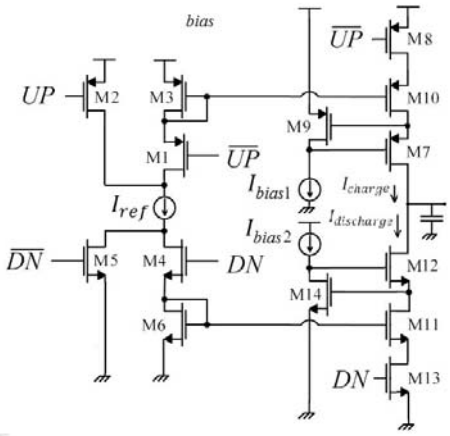


Figure 4. Gain Boosted CP circuit.

Fig. 5 shows a conventional bulk driven current mirror circuit [9]. The gate terminals of transistors are connected to a fixed voltage which is lower than Vdd to develop a moderate inversion layer beneath the gate. The bulk terminal of transistors are connected to a voltage which is higher than their sources. It means that the source bulk voltage (VSB) is decreased. Therefore, according to the following equation, V_T is decreased.

$$V_T = V_{T0} + \gamma(\sqrt{\varphi_F + V_{SB}} - \sqrt{\varphi_F}) \quad (5)$$

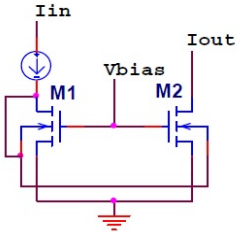


Figure 5. Conventional bulk driven current mirror

By decreasing the value of V_T, the value of power consumption will be decreased, while the value of voltage swing will be increased significantly [8].

Fig. 6 shows the schematic of proposed bulk driven circuit using an adaptive gate bias technique [8]. To obtain a high output impedance in the proposed charge pump circuit, transistors must operate in the saturation region. By applying the adaptive gate bias technique, the transistors will operate in the saturation region in presence of the input current variations. It means that the output impedance does not oscillate and the charge pump current mismatch will be almost omitted.

Bulk driven is performed by making a drain bulk connection for transistors M15-M18, which produce reference voltages for bulk terminals of the output transistors. The gate of these transistors are connected to the gate of the reference current mirror transistors to make an adaptive bias circuit. Therefore, the gate voltages will vary, as Iref changes, without any mismatch in output current. The critical point, in this design, is that making the bulk driven transistors in the border of saturation region. If not, a leakage current will pass through the source bulk junction. The mentioned task is done by choosing the sizes of these transistors accurately. M8 and M13 are used as charge pump circuit switches.

The output impedance of proposed circuit is shown in the following equations.

$$R_{out,dn} = ((gm_{12} + gmb_{12})ro_{12}[(gm_{11} + gmb_{11})ro_{13}ro_{11}](gm_{14}ro_{14}))$$

$$R_{out,up} = ((gm_{7} + gmb_{7})ro_{7}[(gm_{10} + gmb_{10})ro8ro_{10}](gm_{9}ro_{9}))$$

$$R_{tot} = R_{out,up} \| R_{out,dn} \quad (6)$$

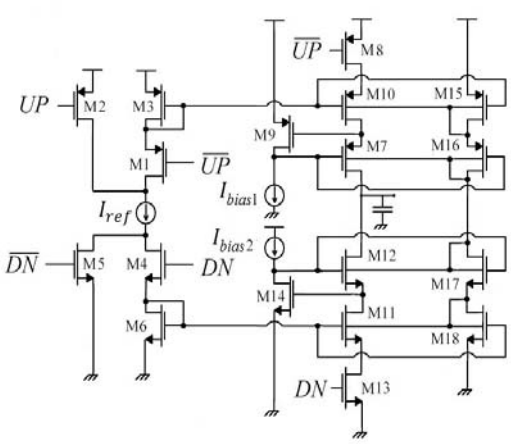


Figure 6. proposed CP circuit

It can be observed that the output impedance is very high, while the values of output swing and power consumption, are completely acceptable.

III. SIMULATION RESULT

The proposed charge pump circuit was simulated, using BSIM model with level49, under HSPICE with 0.18µm, 1.8V CMOS parameters. Fig. 7 shows the variations of the UP/DN current with the proposed gain boosting circuit as the CP output voltage sweeps from 0 to 1.8V. This circuit shows the current matching characteristics less than 0.5% of the sourcing/sinking current difference. Fig.8 (a) and (b) show the charging and discharging process of output node in presence of Up and Down voltages respectively. As can be seen, the charging and discharging process is fast enough and there is no glitch in the output voltage. To evaluate the effect, which are resulting from the fabrication on the circuit performance, the output current variation is simulated using a Mont Carlo process variations simulation. As indicated in Fig.9 the standard derivation is obtained as 0.03% of the nominal 50uA output current. The overall power consumption of the proposed charge pump circuit is around 1.5mW with a 1.8 V supply voltage. A performance comparison of proposed charge pump is stablished in Table 1. In the proposed structure, due to the use of a gain boosting structure, the output impedance becomes very high. Furthermore, because of employing the bulk driven method, the voltage swing is increased while the power consumption is reasonable.

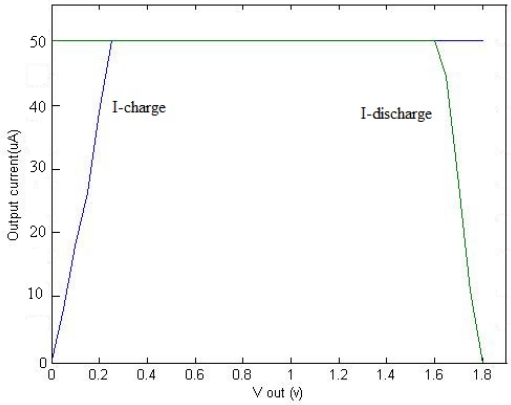
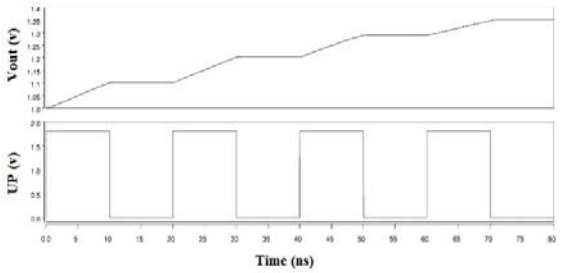


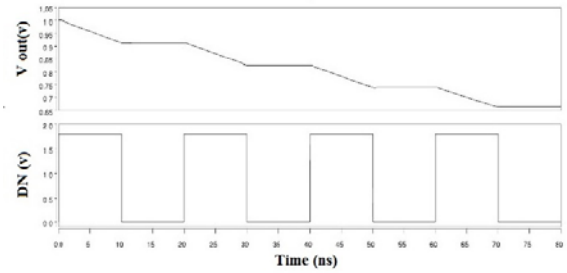
Figure 7. Matching characteristics of the proposed CP

IV. CONCLUSIONS

In this article a gain-boosting CP circuit, with a good current matching characteristic, is proposed. By using a simple gain-boosting circuit, an excellent matching characteristic is achieved. Furthermore, by employing the bulk driven method, the output voltage swing is increased while the power consumption is decreased in comparison with similar gain boosting methods. The overall power consumption of the proposed charge pump circuit is around 1.5mW with a 1.8 V supply voltage.



(a)



(b)

Figure 8. Charging and discharging of the outputs voltage in presents of (a) UP and (b) DN signals

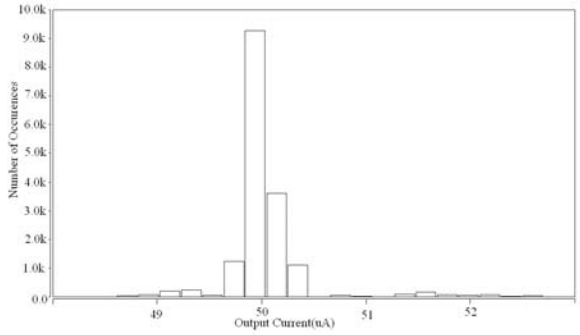


Figure 9. Mont Carlo process variations of the output current as W changes

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TABLE I. A PERFORMANCE COMPARISON OF PROPOSED CHARGE PUMP CIRCUIT

	[4]	[8]	[1]	[10]	Propsed Circuit
CMOS Process(µm)	0.13	0.18	0.18	0.18	0.18
Power Supply(V)	1.2	1.8	1.8	1.8	1.8
Voltage Swing(V)	0.2-1	0.3-1.58	0.5–1.2	0.4-1.25	0.3-1.6
Voltage Swing/Vdd(V)	0.66%	71%	%38	47%	0.72%
Power Consumpton(µW)	NA	395	NA	3100	1460
Outpur Resistance	Moderate (Cascode)	Moderate (Cascode)	Very High (Gain Boosting)	High (Improved Cascode)	Very High (Gain Boosting)