A NEW CURRENT MODE HIGH SPEED FOUR QUADRANT CMOS ANALOG MULTIPLIER

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Abstract— **In this paper current mode analog CMOS multipliers are shortly reviewed and categorized. Then a new current mode four-quadrant analog multiplier circuit is proposed. The new circuit structure is based on trans-linear loops and employs three new compact squaring circuits. Simpler circuit structure, lower power dissipation, lower THD and higher bandwidth are some advantages of the proposed multiplier and also the input resistance is independent of the input current. Post layout simulation results of the multiplier using Cadence Spectre and Asura in 0.18µm standard CMOS technology shows a THD of 1.01% (@1MHz), a -3dB bandwidth of 840 MHz, and a power consumption of 89.2 µW.**

Keywords- current mode, trans-linear loops, analog multiplier, four quadrants.

I. INTRODUCTION

Multipliers have many applications in analog systems and circuits. Modulator and mixer in communication systems are early applications of this block [1]. Newer applications of this block are usage in implementing neural network and fuzzy logic systems[1]-[2]. In a general point of view, we can classify multipliers in two categories of voltage and current. Current mode processing has more advantages than voltage mode. These advantages include wider bandwidth, more linearity, lower power dissipation, simpler circuitry and so on [3]. In [1], MOS voltage mode multipliers are classified in eight categories according to transistor region of operation, nonlinearity cancellation schemes, and signal injection method. But this classification doesn't include current mode multipliers.

Most of current mode multipliers which are implemented in transistor level can be divided in two categories of strong inversion ([4]-[17]) and weak inversion([18]-[21]). Although there are multipliers which are proposed based on blocks like OTA ([24]), CCII ([25]-[27]) and different types of CDTAs and its derivatives([28]-[33]). But most of these use BJT transistors and aren't optimized in the term of power dissipation and area consumption.

Despite the low power dissipation of multipliers in weak inversion region, linearity and bandwidth aren't desirable. Current mode multipliers that operate in strong inversion can be divided in two categories:

1. Multipliers that have been designed based on geometric mean and squaring/dividing blocks ([4]-[7])(figure 1).

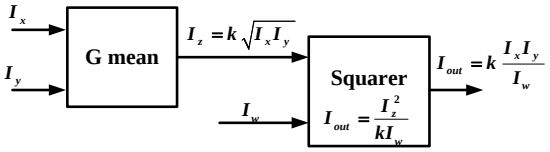
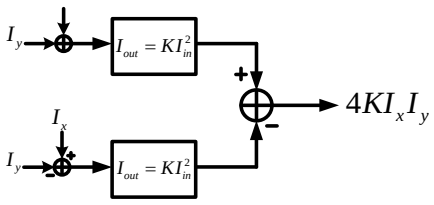


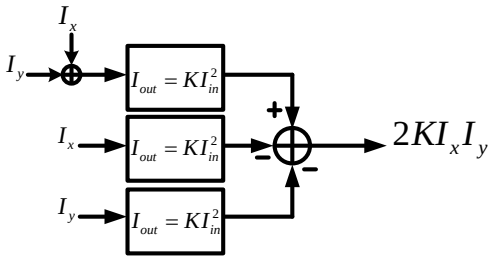
Figure 1 Multipliers that use Geometric mean and Squaring/Dividing block

2. Multipliers that use two or three squaring blocks ([9]-[17]) (figure 2).



$$K\left(I_x + I_y\right)^2 - K\left(I_x - I_y\right)^2 = 4KI_xI_y$$

(*a*)



$$K\left(I_x + I_y\right)^2 - KI_x^2 - KI_y^2 = 2I_xI_y$$

(*b*)

Figure 2 Multipliers that use two or three Squaring blocks

Circuits of the first category only can act as a one quadrant Multiplier but the second are often able to implement a four-quadrant multiplier. Block diagrams of figure 1 and figure 2 have been implemented by two methods of trans-linear scheme ([4]-[7], [9]-[14]) and non-trans-linear scheme([8], [15]-[17]). Non-trans-linear multipliers use various schemes for implementing multiplication function. Dependence on circuit parameters and supply voltage are main disadvantages of non-trans-linear multipliers; also approximation is used for realization of some of them. Trans-linear multipliers don't have these problems and have pure current relation in their output. Table I summarizes our review in current mode multipliers.

Table I summary of multiplier classification

Multiplier type			Implementation	Comment	Ref.
CMOS	Weak Inversion	--	Trans-linear loops	Poor linearity and low BW	[18]-[23]
	Strong inversion	G-mean & squaring circuit	Trans-linear loops	1 Quadrant	[4]-[7]
			Non-Trans-linear loops	1 Quad. /use approximation	[8]
		Squaring circuits	Trans-linear loops	1 or 4 Quadrant	[9]-[14]
			Non-Trans-linear loops	4 Quadrant/ Dependence on Device parameters and supply voltage	[15]-[17]
Non-CMOS (BJT)			OTA, CCII, CDTA ,..	High power dissipation and area consumption	[24]-[33]

In this paper a novel current-mode multiplier design is presented, based on three trans-linear squaring. Its main features are simplicity, precision, high linearity, high band width and low power consumption. The paper organized as follows: In section II circuit design of the proposed multiplier is explained. Simulation results are presented in section III and some conclusions are provided in section IV.

II. CIRCUIT DESIGN

A. Squaring circuit

Figure 3 shows the proposed squaring circuit. This circuit is based on presented circuit in [11] but with essentially different structure. In this circuit M1 and M2 are biased in fixed currents and fixed Gate-Source voltages. Simple current mirror is used for transferring output current, which has wider band-width than the other current mirrors. In Figure 3, transistors M1-M4 form a trans-linear loop. Assuming $V_{TH,N} = |V_{TH,P}| = V_{TH}$ and $K_N = K_P = K$ we have:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \qquad (1)$$

Considering figure 3 we have:

$$I_{D1} = I_{D2} = I_B\ ,\quad I_{D3} = I_o - I_{in}\quad ,\quad I_{D4} = I_o \qquad (2)$$

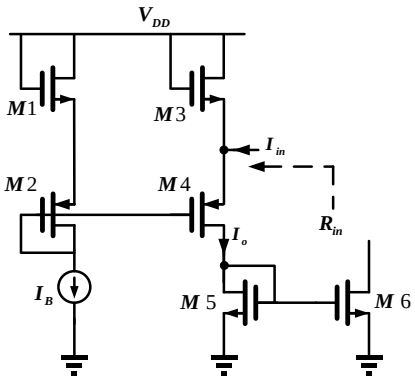


Figure 3 Proposed Two-Quadrant Squaring circuit

By Instating (2) in (1), we have:

$$2\sqrt{I_B} = \sqrt{I_o - I_{in}} + \sqrt{I_o} \qquad (3)$$

By twice squaring and rearranging both sides of (3), it can be written as:

$$I_o = \frac{I_{in}^2}{16\,I_B} + I_B + \frac{I_{in}}{2} \qquad (4)$$

Equation (4) indicates that figure 3 shows squaring circuit which its output is squared of input and has a quiescent current plus a portion of input current.

B. Multiplier circuit

Figure 4 shows the proposed multiplier based on this squaring circuit. This multiplier consists of the five pair of serried transistors (M1-M2, M3-M4, M5-M6, M7-M8 and M9-M10).

(M1-M2) pair constructs four squaring circuits with other 4 pairs. As indicated in figure 4, no signal is applied to the first squaring circuit (M1-M2-M3-M4).

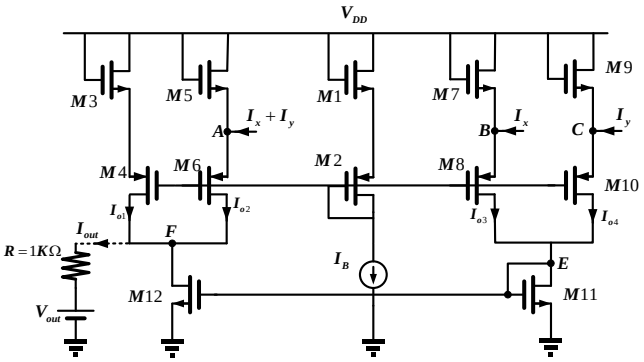


Figure 4 complete circuit of proposed multiplier

According to figure 4 output currents of each squaring circuit will be equal to:

$$I_{o1} = I_B \tag{5}$$

$$I_{o2} = \frac{\left(I_x + I_y\right)^2}{16I_B} + \frac{I_x + I_y}{2} + I_B \tag{6}$$

$$I_{o3} = \frac{I_x^2}{16I_B} + \frac{I_x}{2} + I_B \tag{7}$$

$$I_{o4} = \frac{I_y^2}{16I_B} + \frac{I_y}{2} + I_B \tag{8}$$

Finally, output current is equal to:

$$I_{out} = I_{o1} + I_{o2} - (I_{o3} + I_{o4}) = \frac{I_x I_y}{8I_B} \tag{9}$$

III. PERFORMANCE ANALYSIS

A. *Input range*

From saturation condition of the transistors in the TL in figure 3 we have:

$$|I_{in}| \leq 4I_B \tag{10}$$

This constraint can be easily applied to the multiplier circuit:

$$\begin{aligned} &|I_x + I_y| \leq 4I_B \\ &|I_x| \leq 4I_B \\ &|I_y| \leq 4I_B \end{aligned} \tag{11}$$

Therefore, each input currents are restricted to independently. By proper design of the multiplier we could achieve the input range of twice the bias current.

B. *Input Resistance*

The input resistance of the proposed squaring circuit (multiplier) is derived. This input resistance is indicated in figure 3 as (R_{in}). Input voltage of the squaring circuit (V_{in}) can be derived simply as follows:

$$V_{in} = V_{DD} - V_{TH} + \sqrt{\frac{\left(I_{in} - 4I_B\right)^2}{16KI_B}} \tag{12}$$

From equation (12) the input resistance of the circuit can be derived as follows:

$$R_{in} = \frac{\partial V_{in}}{\partial I_{in}} = \frac{1}{4\sqrt{KI_B}} \tag{13}$$

Equation (13) indicates that the input resistance of the circuit is independent of input currents. This equation is applicable for all squaring circuits that used in the multiplier circuit.

C. *V_{TH} MISSMATCH*

The body-source voltage of a MOS transistor affects the threshold voltage by the equation (14):

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_b + V_{SB}} - \sqrt{2\phi_b}\right) \tag{14}$$

This affect can be cancelled out using twin well or triple well technologies but these technologies are more expensive than NWELL technology. In the proposed circuit NWELL technology has been used therefore all PMOS bodies are tied to their source and all NMOS bodies are tied to ground. Nevertheless if threshold voltages of NMOS transistors varied or a V_{TH} mismatch occurred between N type and P type transistors, the output current of (M1-M2-M3-M4) squaring circuit would be equal to:

$$I_o = \frac{I_{in}^2}{16I_B\left(1 + \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma\right)} + \frac{I_B}{1 + \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma} + \frac{\sqrt{KI_B}\sigma}{1 + \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma} + \frac{I_{in}}{2\left(1 + \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma\right)} + \frac{I_{in}\sigma}{4\sqrt{I_B}\left(1 + \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma\right)} \tag{15}$$

Where:

$$\sigma = V_{TH,NMOS1} + |V_{TH,PMOS1}| - \left(V_{TH,NMOS2} + |V_{TH,PMOS2}|\right) \quad (16)$$

If $|\sigma| << 1$ we can use approximation $\frac{1}{1+\sigma} \approx 1-\sigma$:

$$I_o = \left(\frac{I_{in}^2}{16I_B} + I_B + \sqrt{KI_B}\sigma + \frac{I_{in}}{2} + \frac{I_{in}\sigma}{4\sqrt{I_B}}\right) \times \left(1 - \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma\right) \quad , \quad |\frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma| << 1 \quad (17)$$

Neglecting terms contain σ^2, equation (17) can be rewritten as:

$$I_o = \left(\frac{I_{in}^2}{16I_B} + I_B + \frac{I_{in}}{2}\right)\left(1 - \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma\right) + \frac{I_{in}\sigma}{4\sqrt{I_B}} + \sqrt{KI_B}\sigma \quad , \quad |\frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma| << 1 \quad (18)$$

Applying (18) to each trans-linear loop in figure 4, output current of each squaring circuit would be equal to:

$$I_{o1} = I_B\left(1 - \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma_1\right) + \sqrt{KI_B}\sigma_1 \quad (19)$$

$$I_{o2} = \left(\frac{\left(I_x + I_y\right)^2}{16I_B} + I_B + \frac{I_x + I_y}{2}\right)\left(1 - \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma_2\right) + \frac{\left(I_x + I_y\right)\sigma_2}{4\sqrt{I_B}} + \sqrt{KI_B}\sigma_2 \quad (20)$$

$$I_{o3} = \left(\frac{I_x^2}{16I_B} + I_B + \frac{I_x}{2}\right)\left(1 - \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma_3\right) + \frac{I_x\sigma_3}{4\sqrt{I_B}} + \sqrt{KI_B}\sigma_3 \quad (21)$$

$$I_{o4} = \left(\frac{I_y^2}{16I_B} + I_B + \frac{I_y}{2}\right)\left(1 - \frac{1}{2}\sqrt{\frac{K}{I_B}}\sigma_4\right) + \frac{I_y\sigma_4}{4\sqrt{I_B}} + \sqrt{KI_B}\sigma_4 \quad (22)$$

Where σ_i is the threshold voltage mismatch of transistors in i'th squaring circuit as indicated in equation (16). Finally, output current of multiplier considering produced errors can be rewritten as:

$$I_{out} = \frac{I_x I_y}{8I_B} + \sum_{i=1}^{6} E_i \quad (23)$$

Where:

$$E_1 = \left(\sqrt{KI_B} - \frac{1}{2}\sqrt{\frac{K}{I_B}}\right)\left(\sigma_1 + \sigma_2 - \sigma_3 - \sigma_4\right) \quad (24)$$

$$E_2 = \frac{I_x}{4\sqrt{I_B}}\left(1 - \sqrt{K}\right)\left(\sigma_2 - \sigma_3\right) \quad (25)$$

$$E_3 = \frac{I_y}{4\sqrt{I_B}}\left(1 - \sqrt{K}\right)\left(\sigma_2 - \sigma_4\right) \quad (26)$$

$$E_4 = \frac{I_x^2}{32I_B}\sqrt{\frac{K}{I_B}}\left(\sigma_3 - \sigma_2\right) \quad (27)$$

$$E_5 = \frac{I_y^2}{32I_B}\sqrt{\frac{K}{I_B}}\left(\sigma_4 - \sigma_2\right) \quad (28)$$

$$E_6 = -\frac{I_x I_y}{16I_B}\sqrt{\frac{K}{I_B}}\sigma_2 \quad (29)$$

In these equations, E1 is a DC error. It can be reduced by simple changing of bias current. Also if $\sigma_1=\sigma_2=\sigma_3=\sigma_4$, then the only remaining error would be E6.

D. Trans-conductance Parameter Mismatch

The mismatch of the trans-conductance parameters can be modeled as follows:

$$K_{PMOS} = K(1+\frac{\delta}{2}) \quad , \quad K_{NMOS} = K(1-\frac{\delta}{2}) \quad , \quad \delta << 1 \quad (30)$$

By rewriting trans-linear equation for TL of figure 3, it can be deduced:

$$\sqrt{\frac{I_B}{K\left(1-\delta/2\right)}} + \sqrt{\frac{I_B}{K\left(1+\delta/2\right)}} = \sqrt{\frac{I_o}{K\left(1-\delta/2\right)}} + \sqrt{\frac{I_o - I_{in}}{K\left(1+\delta/2\right)}} \quad (31)$$

Where I_{in} and I_o are input current and output currents of TL, respectively. By exerting some mathematic operation and neglecting σ^2 term, equation (31) can be rewritten as:

$$I_o = \frac{I_{in}^2}{16I_B} + I_B + \frac{I_{in}}{2} + \frac{\delta I_{in}}{8} - \frac{\delta I_{in}^2}{16I_B} - \frac{\delta I_{in}^3}{128I_B^2} \quad (32)$$

Applying equation (32) to each trans-linear loop, equation (33) can be gotten:

$$I_{out} = \frac{I_x I_y}{8I_B}(1-\delta) - \frac{3\delta}{128I_B^2}\left(I_x^2 I_y + I_x I_y^2\right) \quad (33)$$

IV. Simulation Results

The performance of circuit has been studied through post layout simulation using Cadence Spectre and Assura by 0.18µm standard CMOS technology. Supply voltage and current are equal to 1.8V and 10µA respectively. Simulated power dissipation for this multiplier is 89.2µW. Output current enters to a 0.6V supply voltage. Table II shows the aspect ratio of the transistors that used in the multiplier of figure 4. Figure 5 shows the layout of the proposed 4 quadrant multiplier where Metal1 and Metal2 are the only layers that have been used. The size of the circuit is 10µm×20µm or 200 µm2.

Table II Dimensions of transistors in figure 4 (Dimensions are in µm)

$(W/L)_{1,3,5,7,9}$	$(W/L)_{2,4,6,8,10}$	$(W/L)_{11,12}$
0.36/0.54	3.24/0.54	2.52/0.36

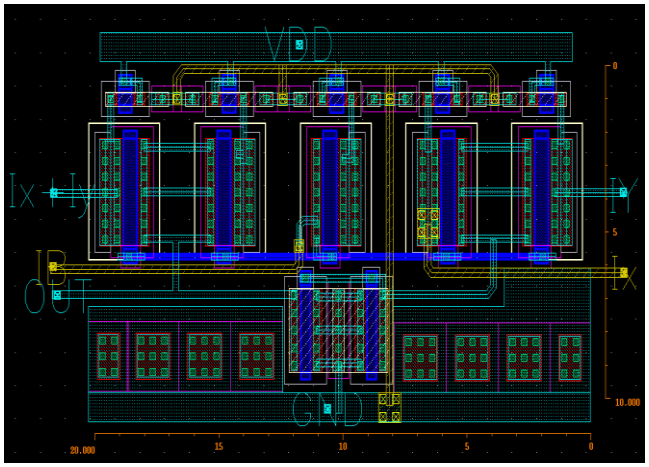


Figure 5 layout of the proposed multiplier

A. *Transient response*

Figure 6 shows the transient output current. Input signals are equal to $I_x = 20\sin(2\pi \times 10^6 t)\,\mu A$ and $I_y = 20\sin(2\pi \times 10^5 t)\,\mu A$ True operation of the multiplier can be deduced from this figure.

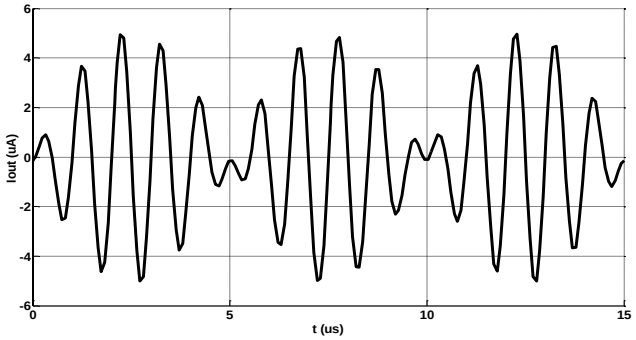


Figure 6 Post layout simulation of Transient response of multiplier

B. *DC analysis*

Figure 7 shows post layout DC analysis of proposed multiplier. Output response is plotted for different I_y's. Monotone slope of lines represents desirable performance of circuit in whole scope range.

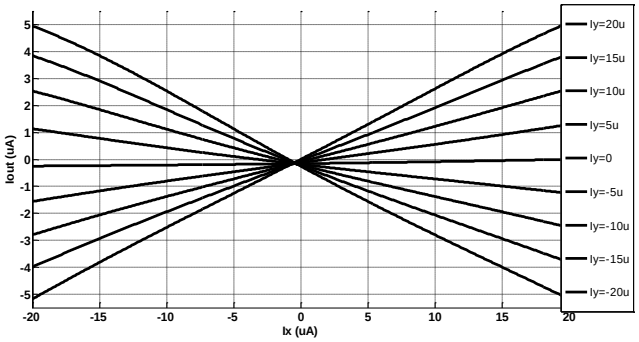


Figure 7 DC response of multiplier for both inputs changes

C. *THD*

Figure 8 shows post layout simulation of THD for different frequencies and different amplitudes. In this figure I_x is set to a sinusoidal signal with variable amplitude and I_y is set to maximum amount of 20 µA DC. Because of symmetrical nature of circuit, the THD for variable I_y and fixed biased Ix is approximately similar to this figure. The THD in 1MHz frequency is as low as 1.01% and higher frequencies like 50 MHz is 5.6%.

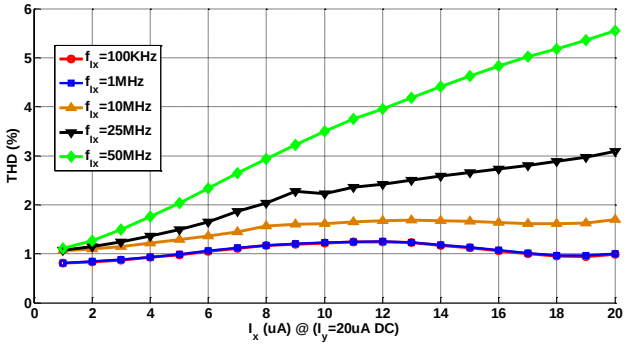


Figure 8 THD of multiplier circuit for different frequencies (I_x is a sinusoidal signal with amplitude of 20 µA)

D. Input Resistance

The input resistance of the multiplier in node A and node B (of figure 4) are simulated in the figure 9. As can be seen in this figure the input resistances have very low dependence of input current.

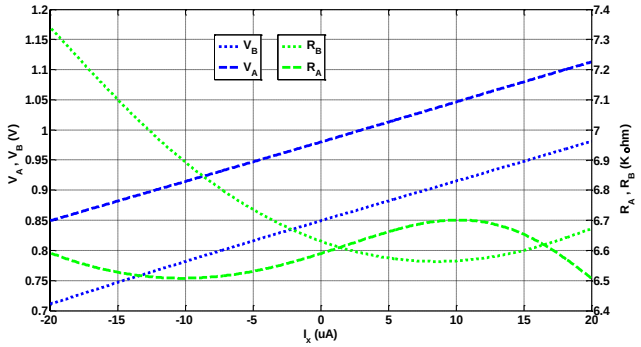


Figure 9 input voltage and input resistance of the nodes A and B of the multiplier versus I_x (I_y=20µA)

E. Frequency response

Post layout simulation of the frequency response of multiplier is shown in figure 10. The post layout simulated BW is about 840 MHz.

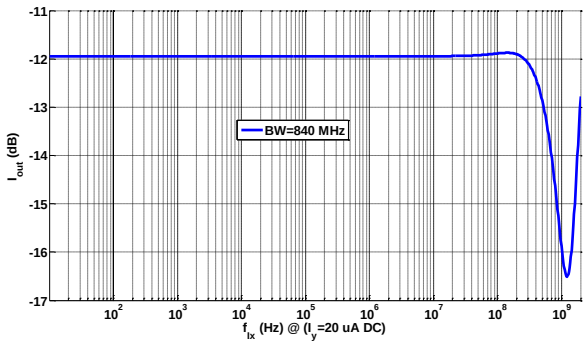


Figure 10 frequency response of multiplier circuit

F. Corner Case Analysis and temperature effect

Figure 11 shows the corner case analysis of small signal response for the TT, SS, FF, SF and FS corners. This figure proves that our proposed multiplier can work even in the worst corners of technology.

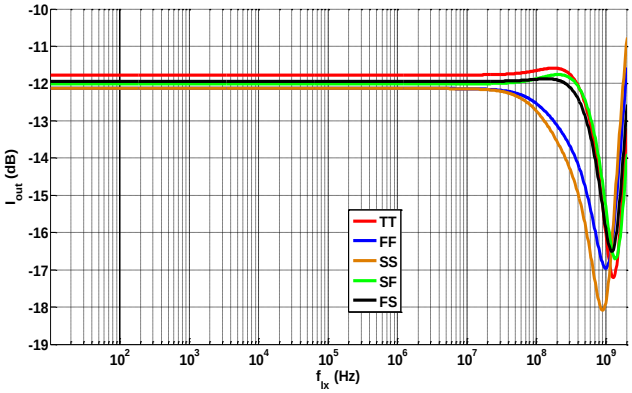


Figure 11 corner case analysis for ac response

Table III shows the variation of THD in the different corners of technology.

Table III corner case analysis of the THD at 1MHz frequency

Technology corner	THD @ 1MHz
TT	1.01
SS	1.21
FF	1.25
SF	1.88
SF	1.7

Figure 12 shows time response of multiplier in various temperatures. It can be seen that the circuit has very low sensitivity to temperature through 100oC temperature variations.

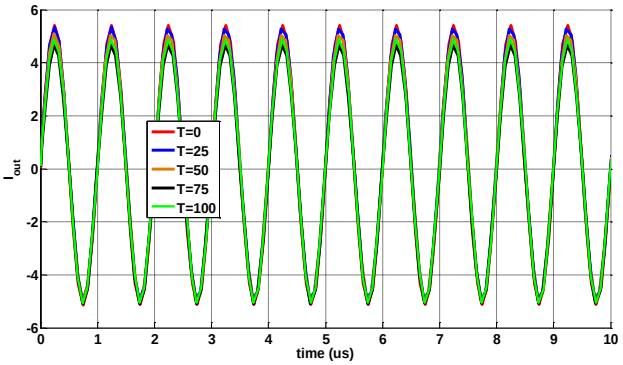


Figure 12 Time response for temperature variations from 0^oC to 100^0C

Table IV shows a comparison between this work and the other reported current mode analog multipliers. For a better comparison, we introduce a figure of merit, FOM, as follows:

$$FOM = \frac{BW[MHz]}{P_{diss}[\mu W].THD[\%]} \cdot \frac{Input\ Range[\mu A]}{Bias\ Current\ [\mu A]} \quad (34)$$

This FOM contains four important parameters of Multipliers. Obviously, the proposed circuit in this work pertains the largest value.

Table IV comparison between this work and other reported circuits

Ref./Year	[11] /2009	[12]* /2012	[16] /2003	[17] /2006	[18] /2005	[19] /2007	[23] /2011	**This work***
Tech. (µm)	0.35	0.25	0.8	0.25	0.35	0.35	0.13	**0.18**
Power (µW)	340	168	390	>250	5.5	9 (Max.)	0.063	**89.2**
THD (%)	0.97 @ 1MHz	0.91@ 1MHz	0.95 @ 1KHz	0.25 @ 1MHz	0.9 @ 1KHz	1 @ 100KHz	3.1 @ 2KHz	**1.01@ 1MHz**
Supply Voltage (V)	3.3	2.5	±0.75	1.5	2	2	0.65	**1.8**
Input range/Bias Current (µA)/ (µA)	±10/10	±10/10	±40/NA[1]	±100/80	±0.25/0.25	±0.1/0.05	±0.04 /0.005	**±20/10**
BW (MHz)	41.8	278	61	154	0.2	19	NA	**840**
N.Q[2]	4	4	4	4	4	4	4	**4**
Area (µm^2)	855	331	4×10^4	NA	1870	NA	NA	**200**
FOM	0.13	1.65	NA	0.77	<0.04	<4.2	NA	**18.83**
Sim/Meas[3]	Sim	Sim	Sim	Meas	Meas	Sim	Sim	**Sim**

[1]Not Available, [2]Number of Quadrants, [3]Simulation or Measurement, *post layout simulation results.

V. CONCLUSION

In this paper analog COMS multipliers are shortly surveyed and categorized. Then a new current mode analog multiplier has been proposed based on MOS trans-linear loops. It employs three new compact squaring circuits. The input resistance of the squaring circuit has very small dependence on the input currents. Post layout simulations show the proposed four quadrant multiplier has remarkable advantages like low harmonic distortion (1.01 @ 1MHz), low power dissipation (89.2µW), high bandwidth (840 MHz) and high input range(20µA per 10µA bias current).

VI. REFERENCES

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