

# A Modified Folded Multi-LSB Decided Resistor String Digital to Analog Converter

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**Abstract**— This work proposes an improved folded multi-LSB decided resistor string digital to analog converter which has lower number of resistors. The nonlinearity calculations are done for this design in order to better analyze the resistor mismatch. Since no buffers are employed to this architecture, the proposed circuit has ameliorated performance in compare with the conventional digital to analog converters. As the buffer is omitted from this topology, the offset problem and the bandwidth limitations are solved.

**Keywords**- digital to analog converter; folded multi-LSB decided; resistor string.

## I. INTRODUCTION

The converters are the main building blocks of the electronic fields especially video processing. Different digital to analog converter (DAC) structures have been designed with various pros and cons. Binary weighted DAC, R-2R ladder DAC, current steering DAC and resistor string DAC are the most common DACs that are used in many applications [1]. Resistor string DAC is one of the first MOS DACs that works based on activating the numbers of switches, which are controlled by digital inputs, and selecting some segmented resistor strings among the total resistors, that shows the analog quantity proportional to the digital input code. Since it needs large number of switches, resistor string DAC with decoder has been presented. By using decoder in the resistor string DAC architecture the number of switches are reduced to  $2^N$ . Despite the best of intentions that it has, the topology of the decoder becomes complicated as the resolution is increased. Therefore the folded resistor string converter was designed that its performance is very similar to that of digital memory [1]. For example in a 4-bit DAC instead of using one 4 to 16 decoder, two 2 to 4 decoders are used. As shown in Fig. 1 each decoder activates one of its four lines. The activation lines of one of the decoders are called word lines while those of other decoder are named bit lines. Each word and bit line activates one transistor and selects one tap of segmented resistors, which is transferred to the analog output [2].

Although the folded resistor string converters reduce the total number of transistors to  $2\sqrt{2^N}$ , the accuracy of the converter is decreased by enhancing the speed [1]. When one of the word lines becomes activated, the bit lines change their

level to a new one and in this situation two or more bit lines are fed to the output buffer.

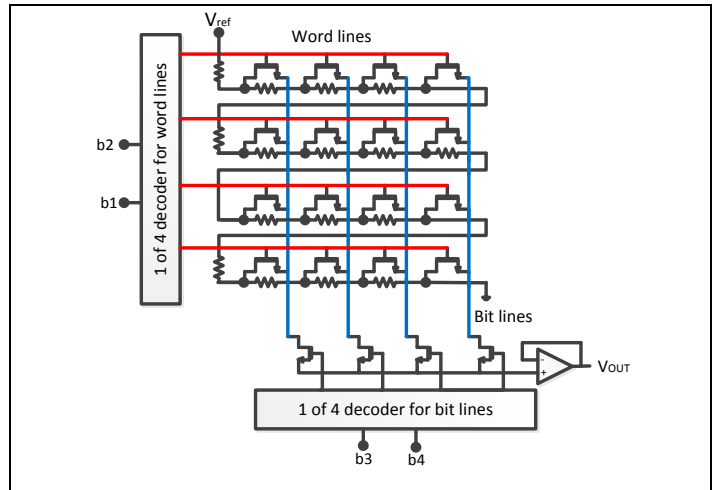


Figure 1. The proposed folded multi-LSB decided resistor string DAC.

To improve the performance of the resistor string DAC an additional interpolating resistor string is employed [3]. The multiple resistor string DAC, if increases the accuracy, has a mismatch problem between two stages. Several methods have been proposed to eliminate the buffer and compensate the effect of interpolator loading on the coarse stage. Buffer resistors which replace the buffer amplifiers, although improve the speed and chip area, require additional control switches [4].

By employing current source isolation technique, the extra logic for controlling the switches of buffer resistors is eliminated, but still there is the mismatch limitation in sinking and sourcing currents [5]. Offset switching technique can also ameliorate the resistance of the switch and capacitive loading effect on the coarse stage, but it can't preferably isolate coarse resistor string from the interpolating resistor stage [3]. Level shifters in the multiple resistor string DAC not only capacitively isolate two resistor stages, but also significantly reduce the ohmic resistance of the switches [3]. Drain- source voltage matching of the NMOS and PMOS transistors in the level shifters is the drawback of this topology.

Folded multi-LSB decided resistor string DAC uses main and sub-resistors in one stage to ameliorate the isolating

requirement between coarse and interpolating resistor string [6, 7]. In this work a modified folded multi-LSB decided DAC is proposed which has lower number of resistors than the conventional ones. The analysis of differential non-linearity (DNL) and integral non-linearity (INL) are discussed for the proposed DAC.

This paper is organized as follows. The modified folded multi-LSB decided resistor string DAC is proposed in section II. DNL and INL calculations are presented in section III and finally section IV concludes the whole work.

## II. A MODIFIED FOLDED MULTI-LSB DECIDED RESISTOR STRING DAC

The proposed design of DAC is shown in Fig. 2. As it is shown in this structure the main resistor string is connected to the analog multiplexer, while the sub-resistor string is activated with the  $L-2^L$  decoder. Since only one sub-resistor string is activated by the decoder, the number of resistors is more decreased in this architecture in compare with the conventional folded multi-LSB decided resistor string DAC. There are  $2^L$  sub-resistors, which provide the appropriate path with switches connected to the  $L-2^L$  decoder. The main resistor string includes  $2^M - 1$  resistors that their values are  $2^L$  times more than those of sub-resistors. The number of required switches for this topology is  $2^{L+1}$  that the NMOS transistors are selected for providing the path for LSB-decided resistors.

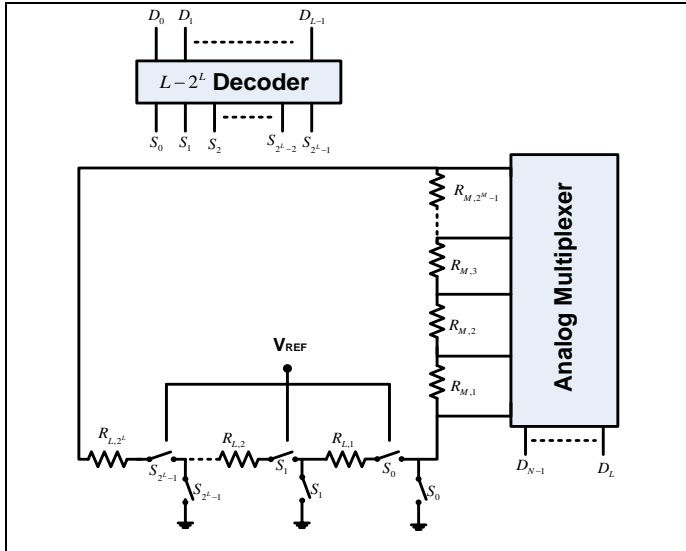


Figure 2. The proposed folded multi-LSB decided resistor string DAC.

For the 4-bit DAC, two schematic are illustrated in Fig. 3 in the case of  $L=2$  and  $L=1$ . In Fig. 3(a) two bits are considered as LSB, therefore  $2^3$  switches and 4 resistors in sub-resistor string are needed. The main resistor string contains three resistors connected to the 2-bit analog multiplexer. It should be noted that the value of the main resistors is four times more than that of sub-resistors. Two LSB and two MSB bits provide the appropriate path to the analog output. If one bit is decided for

LSB, the structure is changed into Fig. 3(b). The number of required switches equals to 4, while only 2 sub-resistors exist in the bottom resistor string. There are  $2^3 - 1 = 7$  main resistors that are fed to the 3-bit analog multiplexer. In this situation the value of main resistors is two times more than the sub-resistors value. It is absolutely certain that by considering  $L=0$  the conventional resistor string DAC is achieved.

The proposed DAC not only reduces the number of resistors and consequently chip area, but also decreases the number of output nodes conducted to the analog output of the resistor string DAC.

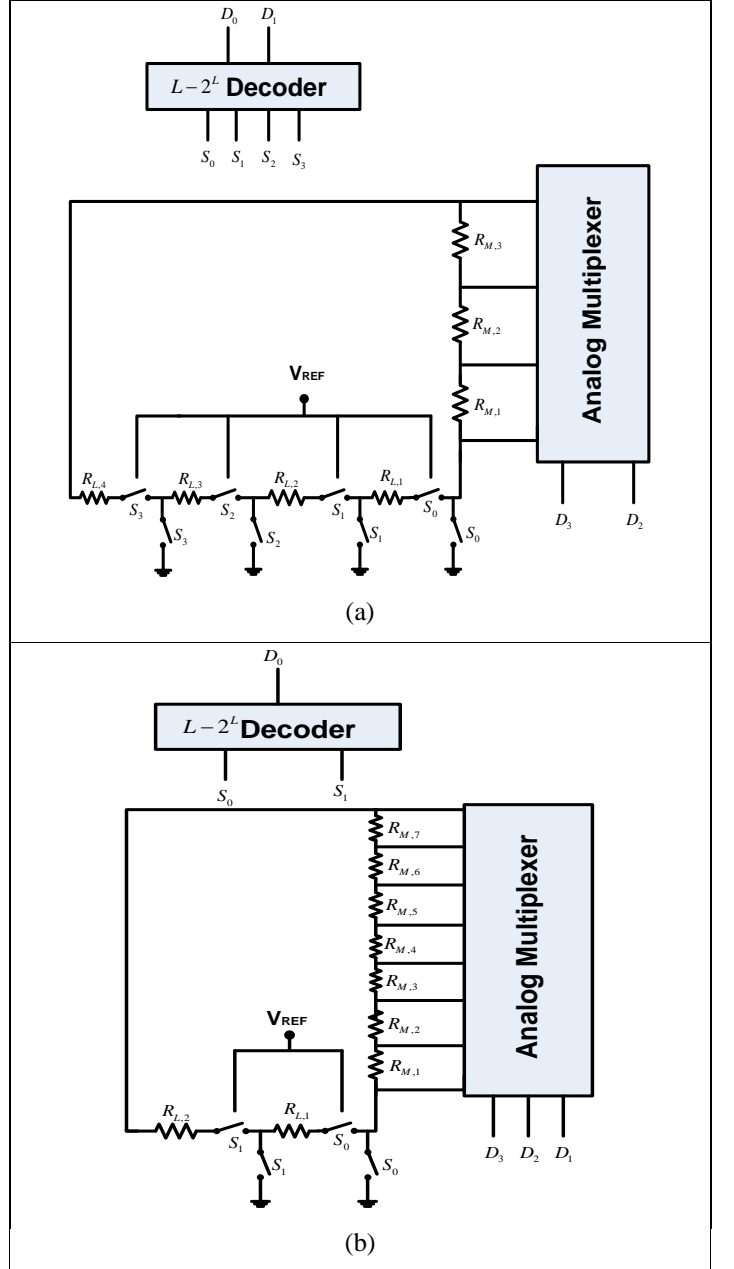


Figure 3. The proposed DAC architecture for (a)  $L=2$ , (b)  $L=1$ .

### III. DNL AND INL EVALUATION

The linearity evaluation is one of the critical parameters that the designers should pay attention for the best DAC performance. DNL and INL are two criteria for linearity analysis.

#### A. DNL Evaluation

DNL is the voltage level difference between the two consecutive actual analog output voltages and one LSB voltage [8]. It should be noted that for the best design DNL must be lower than the half of  $V_{LSB}$ . The worst DNL is gained when the MSB transition takes place from 0 to 1, while the other bits have the vice versa transition. Therefore the DNL can be calculated as (1):

$$V_o(10...0) - V_o(01...1) - V_{LSB} \leq \frac{V_{LSB}}{2} \quad (1)$$

where

$$V_o(10...0) = \left( \frac{2^{M-1}R + \sum_{i=1}^{2^{M-1}} \Delta R_{M,i}}{2^M R + \sum_{i=1}^{2^M-1} \Delta R_{M,i} + \frac{1}{2^L} \sum_{j=1}^{2^L} \Delta R_{L,j}} \right) \quad (2)$$

$$V_o(01...1) = \left( \frac{\left(2^{M-1} - \frac{1}{2^L}\right)R + \sum_{i=1}^{2^{M-1}-1} \Delta R_{M,i} + \frac{1}{2^L} \sum_{j=1}^{2^L-1} \Delta R_{L,j}}{2^M R + \sum_{i=1}^{2^M-1} \Delta R_{M,i} + \frac{1}{2^L} \sum_{j=1}^{2^L} \Delta R_{L,j}} \right) \quad (3)$$

To use Taylor's series, equations (2) and (3) are simplified and the DNL is achieved as follow:

$$\left[ \frac{\frac{1}{2} + \frac{1}{2^M} \sum_{i=1}^{2^{M-1}} \frac{\Delta R_{M,i}}{R}}{1 + \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} + \frac{1}{2^L} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R}} - \frac{\left( \frac{1}{2} - \frac{1}{2^N} + \frac{1}{2^M} \sum_{i=1}^{2^{M-1}-1} \frac{\Delta R_{M,i}}{R} + \frac{1}{2^L} \sum_{j=1}^{2^L-1} \frac{\Delta R_{L,j}}{R} \right)}{1 + \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} + \frac{1}{2^L} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R}} - \frac{1}{2^N} \right] V_{REF} \leq \frac{V_{REF}}{2^{N+1}} \quad (4)$$

After using the approximation of Taylor's series, (4) can be rewritten as:

$$\left\{ \left( \frac{1}{2^N} + \frac{1}{2^M} \sum_{i=2^{M-1}}^{2^M-1} \frac{\Delta R_{M,i}}{R} - \frac{1}{2^L} \frac{1}{2^M} \sum_{j=1}^{2^L-1} \frac{\Delta R_{L,j}}{R} \right) \left[ 1 - \left( \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} + \frac{1}{2^L} \frac{1}{2^M} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R} \right) \right] - \frac{1}{2^N} \right\} V_{REF} \leq \frac{V_{REF}}{2^{N+1}} \quad (5)$$

The equation (5) is simplified as (6):

$$\left( \frac{1}{2^M} \sum_{i=2^{M-1}}^{2^M-1} \frac{\Delta R_{M,i}}{R} - \frac{1}{2^L} \frac{1}{2^M} \sum_{j=1}^{2^L-1} \frac{\Delta R_{L,j}}{R} - \frac{1}{2^N} \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} - \frac{1}{2^N} \frac{1}{2^L} \frac{1}{2^M} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R} \right) V_{REF} \leq \frac{V_{REF}}{2^{N+1}} \quad (6)$$

The probability of (6) can be calculated as (7), due to the fact that  $\Delta R$  is normally distributed.

$$P \left\{ \frac{1}{2^{N+M}} \left( \overbrace{2^N \sum_{i=2^{M-1}}^{2^M-1} \frac{\Delta R_{M,i}}{R} - 2^{N-L} \sum_{j=1}^{2^L-1} \frac{\Delta R_{L,j}}{R}}^X - \overbrace{\sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} - 2^{-L} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R}}^X \right) \geq Y \right\} \quad (7)$$

where Y is the yield and  $0 < Y < 1$ . Thus the variance of X can be measured as (8).

$$\sigma_X^2 \equiv \frac{\sigma_{\Delta R}^2}{2^{2(N+M)}} \left[ 2^{2N} \sum_{i=2^{M-1}}^{2^M-1} 1 + 2^{2N} 2^{-2L} \sum_{j=1}^{2^L-1} 1 + \sum_{i=1}^{2^M-1} 1 + 2^{-2L} \sum_{j=1}^{2^L} 1 \right] \quad (8)$$

and the standard deviation of X can be achieved as (9).

$$\sigma_X \equiv \frac{\sigma_{\Delta R}}{2^{(N+M)}} \left[ 2^{2N} + 2^{2N} 2^{-2L} (2^L - 1) + (2^M - 1) + 2^{-L} \right]^{1/2} \quad (9)$$

As  $\Phi$  is the standard normal distribution function, the probability can be gained as (10).

$$P \left\{ X \leq \frac{R}{2^{N+1}} \right\} = \phi \left( \frac{R}{2^{N+1} \sigma_X} \right) \geq Y \quad (10)$$

By replacing equation (9) in (10), the  $\Phi^{-1}$  is calculated as (11).

$$\phi^{-1}(Y) \frac{\sigma_{\Delta R}}{R} \leq \frac{2^{(N+M)}}{2^{N+1} \sqrt{2^{2N} + 2^{2N} 2^{-2L} (2^L - 1) + (2^M - 1) + 2^{-L}}} \quad (11)$$

### B. INL Evaluation

INL is the criterion that can evaluate the actual output deviation of the analog converter from the reference line. Therefore the INL of the DAC is expressed as the difference between the output values of input code  $i$  and  $i \times V_{LSB}$ , while  $i$  changes from 1 to  $2^N - 1$ .

Similar to DNL calculation, the INL is evaluated for the worst case. In other words INL is derived for the midpoint of the resistor string. The proposed DAC has the appropriate performance if its INL is less than  $0.5V_{LSB}$  as follow:

$$V_o(10...0)_{actual} - V_o(10...0)_{ideal} \leq \frac{V_{LSB}}{2} \quad (12)$$

By replacing the related value to each term, equation (13) is achieved.

$$\left[ \frac{2^{M-1} R + \sum_{i=1}^{2^M-1} \Delta R_{M,i}}{2^M R + \sum_{i=1}^{2^M-1} \Delta R_{M,i} + \frac{1}{2^L} \sum_{j=1}^{2^L} \Delta R_{L,j}} - \frac{1}{2} \right] V_{REF} \leq \frac{V_{REF}}{2^{N+1}} \quad (13)$$

Simplifying (13), equation (14) is gained.

$$\left[ \frac{\frac{1}{2} + \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R}}{1 + \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} + \frac{1}{2^L} \frac{1}{2^M} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R}} - \frac{1}{2} \right] V_{REF} \leq \frac{V_{REF}}{2^{N+1}} \quad (14)$$

Using Taylor's series (14) is approximated with (15).

$$\left( \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} \right) \left[ 1 - \left( \frac{1}{2^M} \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} + \frac{1}{2^L} \frac{1}{2^M} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R} \right) \right] V_{REF} \leq \frac{V_{REF}}{2} \quad (15)$$

In this case the probability of INL can be calculated as (16).

$$P \left\{ \frac{1}{2^{M+1}} \left( \overbrace{2 \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} - \sum_{i=1}^{2^M-1} \frac{\Delta R_{M,i}}{R} - 2^{-L} \sum_{j=1}^{2^L} \frac{\Delta R_{L,j}}{R}}^X \right) \leq \frac{R}{2^{N+1}} \right\} \geq Y \quad (16)$$

The variance and consequently the standard deviation of  $X$  are calculated as follows:

$$\sigma_X^2 \equiv \frac{\sigma_{\Delta R}^2}{2^{2(M+1)}} \left[ 4 \sum_{i=1}^{2^M-1} 1 + \sum_{i=1}^{2^M-1} 1 + 2^{-2L} \sum_{j=1}^{2^L} 1 \right] \quad (17)$$

$$\sigma_X \equiv \frac{\sigma_{\Delta R}}{2^{(M+1)}} \left[ 4(2^{M-1}) + (2^M - 1) + 2^{-L} \right]^{1/2} \quad (18)$$

Finally the inverse standard normal distribution function which represents the resistor mismatch for the acceptable INL is calculated.

$$\phi^{-1}(Y) \frac{\sigma_{\Delta R}}{R} \leq \frac{2^{M+1}}{2^{N+1} \sqrt{3 \times 2^M + 2^{-L} - 1}} \quad (19)$$

## IV. CONCLUSION

The modified folded multi-LSB decided resistor string DAC is proposed in order to decrease the number of resistors. By eliminating the buffer amplifier from the resistor string DACs the offset and speed problems are solved. The non-linearity evaluation is done with details. DNL and INL calculations are presented to analyze the required resistor mismatch in this work. As the number of sub-resistors is diminished in compare with the conventional DACs it can be the best choice for video processing applications.

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