A new differential colpitts divide-by-2 injection locked frequency divider

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Abstract— **In this work, a new differential injection locked frequency divider is proposed. The circuit is realized with a current-switching colpitts voltage controlled oscillator, a NMOS transistor and two inductors. The MOS transistor is used as an injection device for applying the input signal. In the proposed circuit, the MOS transistor is placed between the varactor capacitors. In order to achieve outputs with the division order of two, a second-harmonic input signal is applied to the gate of injection MOS transistor. The proposed ILFD draws 1.702 mA current from 1.5 V supply voltage and locks from 7.45 GHz to 9.25 GHz of input frequency. The divider circuit is designed and simulated with the commercial 0.13µm CMOS technology.**

Keywords- frequency divider; injcetion locking; voltage controlled oscillator; divide-by-2

I. INTRODUCTION

High-speed wide-locking range frequency divider is building block in the communication systems for functions such as frequency synthesis and quadrature signal generation [1]. Recently, there have been introduced different topologies of frequency divider for these purposes and also low power applications. Among different types of frequency dividers such as static, dynamic and injection locking topologies, the later one is more popular for RF systems [2-4]. In fact, due to low power consuming and capability of injection locking based topologies for operating at higher RF frequencies, these types of dividers (ILFDs) have attracted much attention in comparison with the others. The operation mechanism of these topologies is based on injection locking phenomenon. In this case, by injecting an external periodic signal to an oscillator circuit with the free running frequency of ω_o, the oscillator circuit can lock it [5-6]. In fact, if the frequency of injecting signal is very close to the free-running frequency or one of its harmonics, the oscillator will track the input frequency. Generally, each topologies of dividers can be categorized into even and odd mode divisions. Hence, divide-by-2 and divide-by-3 frequency dividers can be adopted in these groups respectively.

Operation mechanism of a divide-by-2 frequency divider

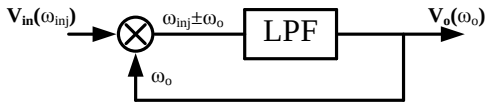

Fig.1 General block diagram of divide-by-2 ILFD

can be modeled with a simple block diagram. In Fig.1, a common model of a divide-by-2 circuit is shown. In this figure, the injection signal is modelled as an additive input (V_{inj}) with a frequency of ω_{inj}. Also, the output frequency is considered as ω_o which is the natural oscillation frequency of the divider when the injected signal is zero. The mixer block in this model achieves $\omega_{inj}\pm\omega_o$ frequency components which only low frequency component ($\omega_{inj}-\omega_o$) can flow through the low-pass-filter. On the other hand, the low-pass-filter block suppresses the high frequency component $\omega_{inj}+\omega_o$.

Generally, the injection locked frequency dividers can be categorized into two groups: ring-oscillator-based and LC-oscillator-based ILFDs. The ring-oscillator-based ILFDs have the large locking range and small chip area but the LC-oscillator-based ILFDs are popular frequency dividers due to their high speed, low-noise and low-power applications [7-18]. In the previously reported works, two types of LC-tank based injection locked frequency dividers have been widely studied. On the other hand, LC-tank based oscillators are widely used as core part in the configuration of injection locked frequency dividers. One of the LC-tank based oscillators which is popularly used as a core block in ILFDs is cross-coupled structure. This type of oscillator has the advantage of simplicity implementation and high startup condition. Another type of LC-tank oscillators is colpitts topology which exhibits better phase noise performance in compared with the cross-coupled one [4]. In the previously reported works, colpitts oscillators are widely studied in RF systems.

In this work, a frequently used configuration of colpitts oscillator which is named current-switching can be used as a core part of the proposed divider. Using of this configuration of

oscillator with the simple structure of injecting elements, a new low-noise and low-power ILFD circuit is introduced. In the next section, the proposed circuit is discussed and then in section 3, its simulation results are provided. Finally, a summary of the important points of this work is provided in section 4.

II. THE PROPOSED DIFFERENTIAL COLPITTS ILFD

Schematic of the proposed injection locked frequency divider (ILFD) is shown in Fig. 2. This circuit is consist of a current-switching colpitts oscillator with a components of a MOS transistor and two inductors. The core oscillator composed of two pair transistors, LC-tank (M_{var} & L) and capacitors C_1 and C_2. All MOS transistors in the core oscillator are chosen p-type, since the 1/f noise of the PMOS is usually lower than the NMOS. Note that, the cross-coupled pair of transistors provides the negative resistance to enhance the start-up condition of oscillating and also, the capacitors $C_{1,2}$ with colpitts transistors $M_{1,2}$ form the positive feedback loop.

As can be seen, the injection signal is being applied by the NMOS transistor which is placed between the MOS varactors (M_{var}). This transistor is basically operates in inversion region which with the MOS varactors form the capacitor of LC-tank. MOS Varactors work in inversion region. By increasing the tuning voltage(V_{tune}), which leads to higher varactor capacitors, the oscillation frequency of the LC resonator decreases. Nothing that, DC gate bias of injection transistor is suitably applied which is not shown in Fig. 2. In this circuit, inductors L_3 and L_4 are used to raise the amplitude of the frequency component at the drain and source of transistor M_{inj} in order to achieve wide locking range. In fact, these inductors show high impedance on the drain and source nodes of M_{inj} at the operating frequency. Also, these elements help to filtering the input noise and hence, the phase noise performance of the circuit will be slightly improved.

The injection transistor (M_{inj}) plays as a mixer to combine injection signal with the frequency of ω_{inj} which is close to the second-harmonic of output components with the fundamental frequency of ω_o. Therefore, the generated components of mixer are $\omega_{inj} - \omega_o$ and $\omega_{inj} + \omega_o$ which the lower component is able to pass and the higher one is filtered out by the LC-tank. In fact, LC tank elements form a low-pass-filter block in this circuit. Note that, gate-source and gate-drain parasitic capacitances of injection transistor M_{inj} has significant effect in the mixing of the applied frequency and the output frequency components.

It is worth mentioning that the drain-source current of the injection transistor consist of fundamental output frequency and higher-order components of it. On the other hand, this circuit can be used as a divide-by-3 too. As has been explained in [11], taylor's series expansion for the drain-source current of injection transistor which contains these frequency components can be expressed as

$$i_{ds} = g_m V_{gs} + \frac{g^1{}_m V^2{}_{gs}}{2!} + \frac{g^2{}_m V^3{}_{gs}}{3!} + \ldots \qquad (1)$$

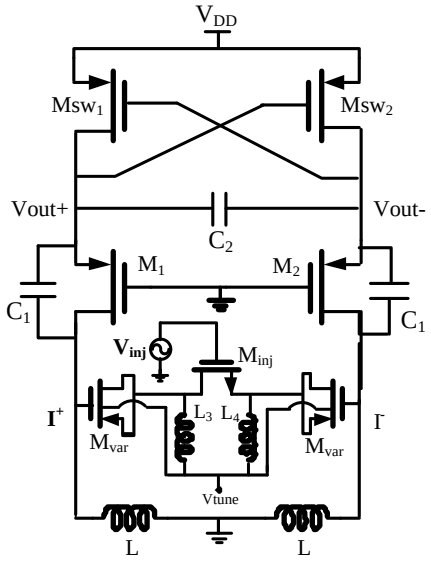

Fig. 2 Schematic of the proposed divide-by-2 ILFD

Where $g^n{}_m$ is the nth order transconductance of injection MOS with respect to the gate-source voltage (V_{gs}). In fact, assuming that the gate-source voltage of injection MOS is given by $V_{GS}\cos(\omega_o t)$, the all frequency components will be observed in this relation. Hence, if the frequency of injection signal will be very close to the second-harmonic or third-harmonic of drain current, the circuit can operate as a divide-by-2 or divide-by-3 ILFD. In divide-by-3 mode of the circuit, the relation between the frequency of input and output is discussed by $\omega_{inj} - 2\omega_o = \omega_o$ which leads to $\omega_o = \omega_{inj}/3$. Note that, when no external signal is injected to the divider circuit, it operates as a differential LC-oscillator with the free running frequency of ω_o. Differential LC-VCOs have symmetric structures which generate two oscillating outputs with the same amplitudes and with half period phase difference between them [8].

In some previously proposed ILFDs as in [12, 15], the injection elements are placed series with transistors of the core oscillator. In this method of injection, the used elements such as MOS transistors require high voltage headroom which limit the amount of the supply voltage. Compared to these works, the injection MOS in the proposed ILFD does not limit the using of this circuit for low voltage applications. Also, compared to the ILFDs in [16, 17], which the injection MOSs are placed parallel with the cross-coupled transistors and add extra current path to the core oscillator, the proposed circuit has another advantage that does not apply additional current to the core oscillator. Hence, the proposed ILFD is suitable for low power applications.

It's worth mentioning that, using the proposed circuit as a divide-by-2 ILFD has larger locking range respect to the dvide-by-3 mode of it. Generally, ILFDs with division order of two show wider locking range compared to the divide-by-3 types of them.

III. SIMULATION RESULTS

The proposed circuit was designed and simulated with the ADS using a standard 0.13-μm RF-CMOS technology. Fig. 3 shows the simulated transient output waveforms of the proposed circuit and it's injection signal with the amplitude of 0.25 V. The operation principle of the proposed divide-by-2 circuit can be understood from this figure. The injection signal with the frequency of $2\omega_o$ is injected, and the transient output with the frequency ω_o is achieved. The output waveform shown in this figure was achieved at V_{DD}=1.5 V and a typical controlling voltage of 0.75 V (V_{tune}=0.75 V). Also, the power consumption of the proposed divide-by-2 ILFD is 2.553 mw.

In Fig. 4, the simulated free running tuning range of the circuit with a fixed gate bias is shown. As can be seen, by varying the varactor tuning voltage from 0 to 1.5 V, the output frequency varies from 3.65 to 4.7 GHz.

According to the simulation, at the incident power of 0dbm the locking range of the proposed circuit is from 7.45 GHz to 9.25 GHz of input frequency. Fig. 5 shows the simulated operation frequency and locking range dependence on input power of the proposed ILFD biased at V_{DD}=1.5 V with V_{tune}= 0 ~ 1.5 V.

Table I shows the comparison of the circuit performances of the proposed ILFD and some previously published reports. It is visible that this proposed work consumes lower power and shows larger locking range.

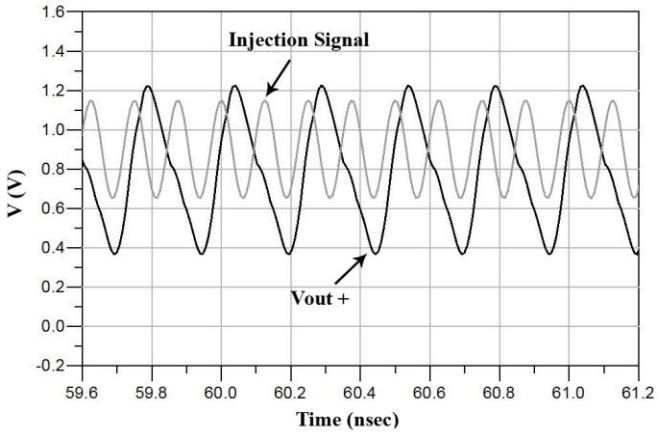

Fig.3 Simulated output waveforms of the proposed circuit for V_{DD} = 1.5V, Vtune = 0.75 V and Vinj=0.25 V

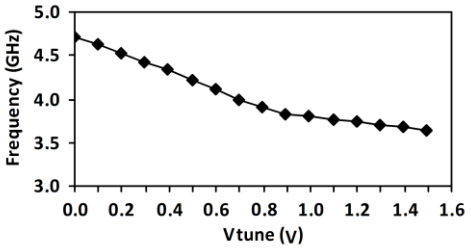

Fig.4 Simulated frequency tuning of the free-running **oscillator** by varying v_{tune} from 0 to 1.5V

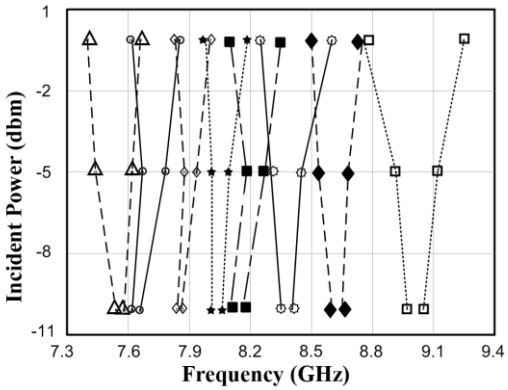

Fig. 5 Simulated input sensitivity of the proposed ILFD at V_{DD} = 1.5 V, from the right to the left, Vtune= 0, 0.2, 0.4, 0.6, 0.8, 1, 1.25, 1.5 V

In Fig.6 the simulated phase noise of the proposed ILFD in the locked condition is shown. The locked phase noise of the divide-by-2 ILFD at 1-MHz offset is -121.55 dBc/Hz, and the phase noise of the injection source at 1-MHz offset is -114 dBc/Hz. The phase noise of the proposed circuit is 7.55 dB lower than the phase noise of the injection source signal.

TABLE I COMPARISON OF THE PERFORMANCES OF THE PROPOSED ILFD WITH THE REPORTED ILFDS IN [9] AND [14]

ILFD	Pin (dBm)	CMOS Tech.	Pdiss. (mw)	Locking Range (GHz)
[9]	-	0.18 μm	4.395	7.512 ~ 8.204
[14]	4	0.18 μm	23	38.3 ~ 40.6
This work (simulated)	0	0.13 μm	2.553	7.45 ~ 9.25

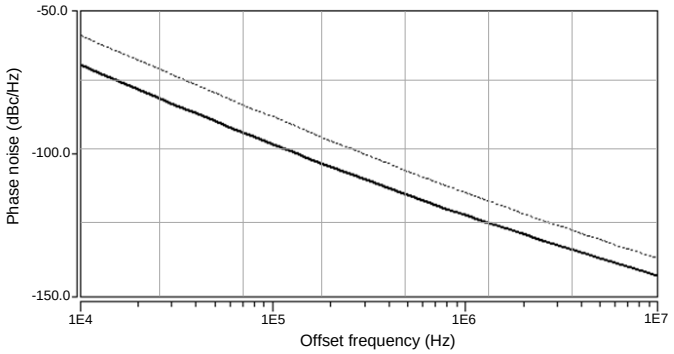

Fig. 6 Simulated phase noises of the injection source and proposed ILFD shown in Fig. 2 at V_{DD}=1.5 V, V_{tune}=0.75 V

IV. CONCLUSION

A new differential colpitts divide-by-2 ILFD has been proposed and simulated in standard 0.13-µm RF-CMOS technology. The proposed circuit is realized with a current-switching colpitts oscillator with a transistor as an injection element and two inductors. The injection transistor which is placed between the varactor capacitors plays as a role of a mixer for the combining of the input injection and the output oscillating signal. Two inductors are used to spread the locking range and lower the phase noise of the circuit. The proposed ILFD consumes 2.553 mw power at the supply voltage of 1.5 V. The locking range of the proposed divide-by-2 circuit is from 7.45 GHz to 9.25 GHz of input frequency at the incident power of 0 dBm. Also, the simulated phase noise of proposed circuit at 1-MHz offset is -121.55 dBc/Hz.

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