A 0.5 V, 112 nW CMOS Temperature Sensor for RFID Food Monitoring Application

Rezvan Dastanian
Assistant Professor
Imam Hussein Faculty of
Engineering
Behbahan Khatam Alanbia
University of Technology
Behbahan, Iran, 6361647189
Email: dastanian@bkatu.ac.ir

Ebrahim Abiri
Associate Professor
Department of Electrical and
Electronics Engineering
Shiraz University of Technology
Shiraz, Iran, 7155713876
Email: abiri@sutech.ac.ir

Mahbubeh Ataiyan
M.Sc
Department of Electrical and
Electronics Engineering
Shiraz University of Technology
Shiraz, Iran, 7155713876
Email: m.ataiyan@sutech.ac.ir

Abstract— **In this paper a low power on-chip temperature sensor, which is appropriate for food monitoring in ultra high frequency radio frequency identification (UHF RFID) passive tag, is proposed. For designing sensor core, MOSFET is used as a temperature sensing element and for decreasing the power consumption, transistors are biased in sub-threshold region. In this sensor for converting the temperature to the digital code, the delay generator and the 9-bit binary counter are utilized. In the design of binary counter, the low power and high speed T flip flap (T-FF) is used in the digital part of sensor, based on gate diffusion input (GDI) technique. The proposed temperature sensor has 38nW power consumption, 0.5V supply voltage and -0.1/0.3 ℃ error due to the Monte Carlo analysis in the temperature range of -10 ℃ to 20 ℃. The simulation is done with Cadence software in 180nm CMOS TSMC Technology, while the chip area is 0.0125mm^2.**

Keywords-: RFID; on-chip temperature sensor; low power consumption; GDI technique; delay generator.

I. INTRODUCTION

Nowadays using of sensor in the RFID tag is developed in order to increase the level of controlling systems. The temperature sensor is one of the RFID sensors which have the science application in controlling the patient temperature [1] and controlling the temperature of the depraving food [2]. The temperature sensors are designed for the various temperatures based on their applications. In these sensors the sensitive element to the temperature can be the resistor [1], BJT transistor [3-6] or MOSFET transistor [2, 7-11]. Among such sensitive elements to the temperature, MOSFETs have the lowest power consumption and acceptable error. To design the sensor, two signals, which are proportional to absolute temperature and complementary to absolute temperature [2] or dependent and independent on the temperature [3-6], should be created in order to measure the temperature with the comparison of these two signals.

The design of sensor with CMOS technology can be categorized into three groups: the temperature sensor based on analog to digital converter (ADC) [3-5], the temperature sensor based on delay propagation and time to digital converter (TDC) [2,6,7] and the temperature sensor based on the ring oscillator and the frequency to digital converter (FDC) [1,10,11] .The

temperature sensor based on the ADC dissipates about 80% of its power in ADC block, while it has high chip area. Therefore, despite the high accuracy, it has high power consumption and chip area which makes it unsuitable for using in RFID applications. Usually two temperature sensors based on ring oscillator and delay propagation are utilized for the purpose of having low chip area and power consumption. In the temperature sensor based on the ring oscillator, the signal which is dependent on the temperature is converted into the frequency and then with the help of FDC the digital data dependent on the temperature is created. In the temperature sensor based on the delay propagation, the signals dependent on the temperature are converted to the delay and then it is changed into the digital data by the TDC. In general, the sensors based on the delay generator and TDC have the lower power consumption and higher accuracy than the sensors based on the ring oscillator and FDC.

In this paper the passive RFID temperature sensor, which has very low power consumption, chip area and error, is proposed. The MOSFET transistors are employed in the core of the sensor as the sensitive element to the temperature and the delay generator with the 9-bit counter, which has 2.5MHz clock frequency, is used for converting temperature to the digital data. The considered temperature range is -10 ℃ to 20 ℃ that is appropriate for temperature controlling of food. In section II the designed temperature sensor is proposed. The simulation results are presented in section III and finally the whole work is concluded in section IV.

II. THE CONFIGURATION OF THE PROPOSED TEMPERATURE SENSOR

Fig. 1 shows the block diagram of the proposed temperature sensor. First, two voltage signals, V_{PTAT} (proportional-to-absolute-temperature) and V_{CTAT} (complimentary-to-absolute-temperature), are generated in the core of the sensor and after passing through the delay generators the modulated temperature signals are converted into the delay signal. The pulse width of PTAT and CTAT delay generator outputs are proportional to the V_{PTAT} value and V_{CTAT} value, respectively. In the next process, these two pulses are used as the inputs of XOR gate. The pulse width of the XOR output is proportional to the voltage difference between V_{PTAT} and V_{CTAT} and it is
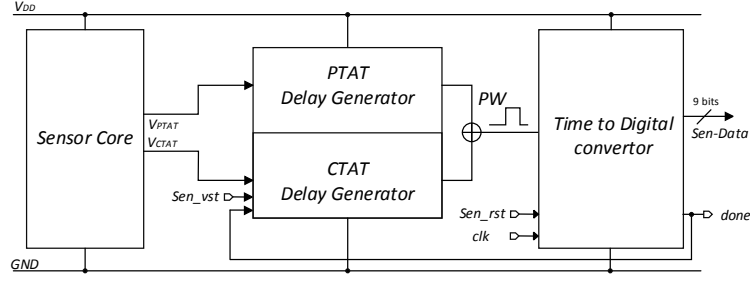
Figure 1. The general block diagram of the proposed temperature sensor of RFID tag

dependent on the temperature. Then, with the binary counter, the output pulse width is countered and it is converted to the digital codes. The converting of the pulse width output to the digital output is done by countering the number of clock edges of the oscillated output along the output pulse width in one sampling period. The sampling period, which is independent of the temperature variation is defined by the RFID reader [9]. Finally, for decreasing the power consumption, the analog part of the sensor becomes off by sending the done signal and then the sensor is provided for the next conversion.

A. The design of the sensor core

For designing the sensor, first PTAT and CTAT signals are produced by the core of the sensor. Fig. 2 (a) shows the presented PTAT voltage generator of Ref. 12. By employing the low supply voltage, transistors work in the sub-threshold region. Based on Fig. 2 (a) PTAT voltage is the voltage difference between the gate- source voltages of M_1 and M_2 transistors which are biased in the sub-threshold region. W/L size of M_1 transistor is k (k>1) times more than that of M_2 transistor. If $V_{ds}>4V_T$, then the drain current of the biased transistor in sub-threshold region is equal to (1).

$$I_{sub} = \mu C_{OX} \left(\frac{W}{L}\right) V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{\eta V_T}\right) \qquad (1)$$

where η is the sub-threshold slope factor, μ is the mobility, C_{ox} is the oxide capacitance per unit area, V_T is the thermal voltage, V_{th} is the threshold voltage, W/L is the transistor sizing and V_{gs} is the gate-source voltage of the transistor.
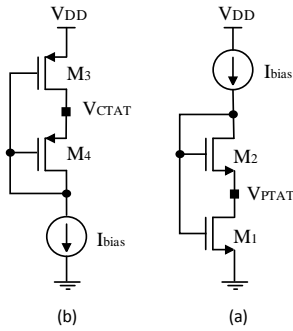

Figure 2. (a) PTAT voltage generator, (b) CTAT voltage generator [12]

Due to the Fig. 2 (a), when MOSFET transistors work in the sub-threshold region, V_{PTAT} is expressed as (2).

$$V_{PTAT} = V_{gs1} - V_{gs2} = \eta V_T \ln k \qquad (2)$$

Fig. 2 (b) shows the CTAT voltage generator, which is the difference between V_{DD} and V_{sg} of M_3 and M_4 transistors biased in the sub-threshold region. Thus, if W/L of M_4 transistor is k´ (k´>1) times more than that of the M_3, CTAT voltage is calculated as (3).

$$V_{CTAT} = V_{DD} - \left(V_{sg3} - V_{sg4}\right) = V_{DD} - \eta V_T \ln k' \qquad (3)$$

where V_{DD} is the supply voltage and V_{sg} is the source-gate voltage of the transistor. The core of the proposed temperature sensor, which includes start-up circuit, nano-ampere current source and PTAT and CTAT signal generators, is shown in Fig. 3. To generate CTAT and PTAT voltages in the proposed sensor core, the primary cores of [12] are cascaded. With the help of such configuration, the PTAT and CTAT voltages are increased more controllably without more increasing of transistors sizes. Based on (2) and (3) and since the value of V_{DD} is low, in order to confluence CTAT and PTAT voltages in the considered temperature range, three and two cascade stages are used respectively for designing CTAT and PTAT cases. Given the fact that M_{P1-4} MOSFET transistors work in the sub-threshold region and the current of M_{P1} transistor is two times more than that of M_{P2}, M_{P3} and M_{P4} transistors, V_{PTAT} is calculated as (4).

$$V_{PTAT} = \left(V_{gs,P1} - V_{gs,P2}\right) + \left(V_{gs,P3} - V_{gs,P4}\right)$$

$$= \eta V_T \ln\left(\frac{I_{P1}}{\mu C_{OX} (W/L)_{P1} V_T^2}\right) - \eta V_T \ln\left(\frac{I_{P2}}{\mu C_{OX} (W/L)_{P2} V_T^2}\right)$$

$$+ \left[\eta V_T \ln\left(\frac{I_{P3}}{\mu C_{OX} (W/L)_{P3} V_T^2}\right) - \eta V_T \ln\left(\frac{I_{P4}}{\mu C_{OX} (W/L)_{P4} V_T^2}\right)\right]$$

$$= \eta V_T \ln\left(\frac{2(W/L)_{P2}.(W/L)_{P4}}{(W/L)_{P1}.(W/L)_{P3}}\right) \qquad (4)$$
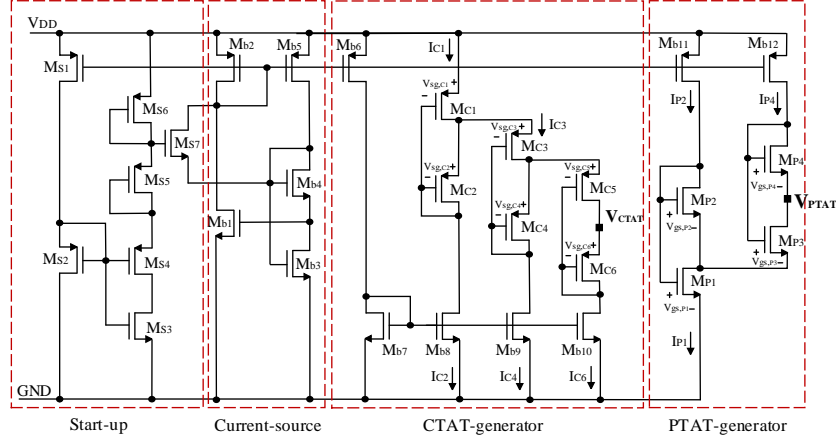
Figure 3. The core of the proposed temperature sensor

Therefore V_{PTAT} is generated with the condition of $2(W/L)_{P2} \cdot (W/L)_{P4} > (W/L)_{P1} \cdot (W/L)_{P3}$ With the similar analysis of V_{PTAT} and by considering the fact that the current of M_{C3} and M_{C4} are respectively two and three times more than that of current source, V_{CTAT} is stated as (5).

$$V_{CTAT} = V_{DD} - \left[\left(V_{sg,C1} - V_{sg,C2} \right) + \left(V_{sg,C3} - V_{sg,C4} \right) + \left(V_{sg,C5} - V_{sg,C6} \right) \right]$$

$$= V_{DD} - \eta V_T \ln \left(\frac{2 \times 3 (W/L)_{C2} \cdot (W/L)_{C4} \cdot (W/L)_{C6}}{(W/L)_{C1} \cdot (W/L)_{C3} \cdot (W/L)_{C5}} \right) \quad (5)$$

Then V_{CTAT} is generated with the condition of $2 \times 3 (W/L)_{C2} \cdot (W/L)_{C4} (W/L)_{C6} > (W/L)_{C1} (W/L)_{C3} \cdot (W/L)_{C5}$.

B. The design of the delay generator

Fig. 4 shows the simple schematic of PTAT and CTAT delay generators, which are connected to the sensor core and the digital part.
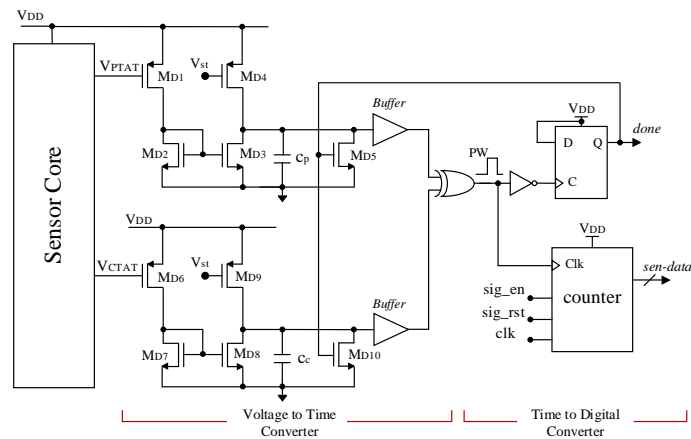
The delay generators of the other papers [2,6] have the voltage level amplified by the Op-Amp and this voltage is employed to the MOSFET transistor gate for converting to the current. Also the resistor is used in such delay generators. Given the fact that the output voltage level of the proposed sensor core is more than that of the other papers, the amplifier isn't employed. As the resistors are no longer used in the proposed design the chip area is reduced.

The modulated temperature voltage signals, V_{PTAT} and V_{CTAT}, which are gained from the core of the sensor, pass through delay generators and are transferred to the time domain. In the CTAT (PTAT) delay generator, M_{D1} (M_{D6}) transistor and $M_{D2,3}$ ($M_{D7,8}$) current mirror transmits V_{PTAT} (V_{CTAT}) to the C_P (C_C) capacitor and the buffer operates as ADC single-slope.

Before each conversion is started, V_{st} signal connects the gate of M_{D4} (M_{D9}) transistor to the ground. In the precharge process, C_P (C_C) capacitor is charged to V_{DD}. The measurement process is started with the rising edge of the clock of V_{st} signal, which is generated by digital core. V_{PTAT} (V_{CTAT}) is employed to the C_P (C_C) capacitor and makes it discharged.

Figure 4. The schematic of the PTAT and CTAT delay generators

At the output of delay generators buffer, the pulses are produced that their width are proportional to the value of PTAT and CTAT voltages and finally these two pulses are employed to the XOR gate. The pulse width of XOR output is calculated as (6).

$$t_{d\text{-}PW}\left(T\right) \approx \frac{C_P \Delta V}{I_{CTAT}\left(T\right)} - \frac{C_C \Delta V}{I_{PTAT}\left(T\right)} \qquad (6)$$

where ΔV is the voltage difference between V_{DD} and the threshold voltage of the buffer transistors. $I_{CTAT}(T)$ and $I_{PTAT}(T)$ are calculated as (7) and (8), respectively.

$$I_{PTAT}\left(T\right) \approx I_{PTAT}\left(T_0\right)\left[1 + k_P\left(T - T_0\right)\right] \qquad (7)$$

$$I_{CTAT}\left(T\right) \approx I_{CTAT}\left(T_0\right)\left[1 - k_C\left(T - T_0\right)\right] \qquad (8)$$

where T is the instantaneous temperature, T_0 is the reference temperature and k_P and k_C are the corresponding proportional constants of I_{PTAT} and I_{CTAT}, respectively. By using (7) and (8) in (6) and by considering only the first and second term, the pulse width of the XOR output is stated as (9).

$$t_{d-PW}\left(T\right) \approx \left[\frac{C_P \Delta V}{I_{CTAT}\left(T_0\right)} - \frac{C_C \Delta V}{I_{PTAT}\left(T_0\right)}\right]$$

$$+ \left[\frac{C_P \Delta V k_C}{I_{CTAT}\left(T_0\right)} + \frac{C_C \Delta V k_P}{I_{PTAT}\left(T_0\right)}\right]\left(T - T_0\right) \qquad (9)$$

It is clear from (9) that if the output pulse width of each delay generator has the nonlinear proportion to the temperature, the pulse width of XOR output omits the nonlinear parts and consequently it has an approximately linear proportion to the temperature. Finally, the counter with the clock generator counts the number of clocks of the output pulse and converts the pulse width into the digital codes. At the end of each conversion, with the falling edge the clock of XOR pulse signal, the done signal is changed and makes C_P and C_C capacitors completely discharged, thus the end of the conversion is distinguished.

C. The design of synchronous T- FF counter with GDI technique

Fig. 5 shows the schematic of 16-transistor T-FF with GDI cell. By using this technique in the structure of T-FF, instead of the 24-transistor CMOS cell, the delay, the number of transistors and the chip area are decreased. By employing this technique to the T-FF, the sub-threshold leakage current and the components of the gate leakage current dissipate lower power than the design with CMOS Flip Flaps. In general, using this Flip Flap in the synchronous binary counter causes more improvement in power dissipation and chip area and consequently the speed of the counter in the digital part of the sensor is increased.

III. SIMULATION RESULTS

The proposed temperature sensor is designed in 180nm CMOS technology. Table 1 presents the sizes of transistors. The output signals of the sensor core. V_{PTAT} and V_{CTAT} are shown in Fig. 6 for the temperature range of -10℃ to 20℃.

Table 1. Summary of transistor sizes of the sensor core

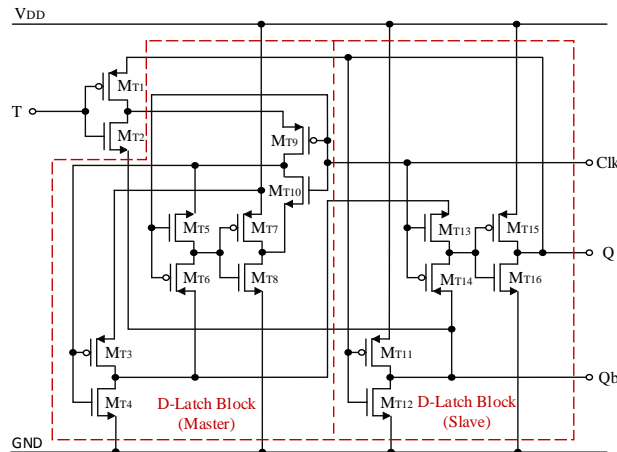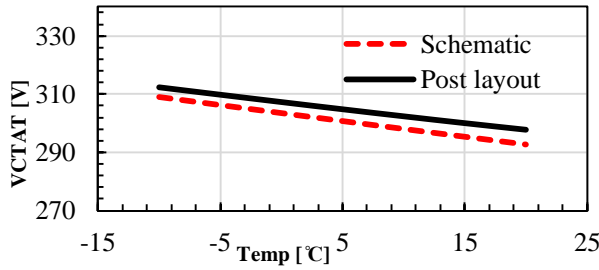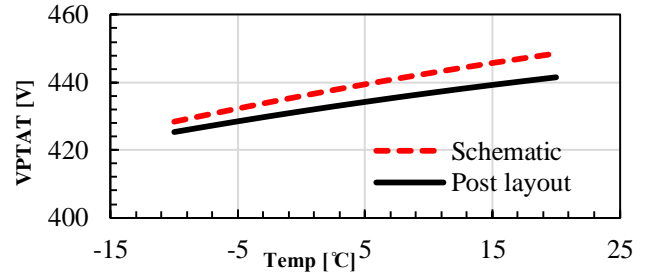| Transistor	W/L [µm/µm]	Transistor	W/L [µm/µm]
M_{b1}	2/0.18	M_{S1-7}	2/0.18
M_{b2-5}	1/0.18	$M_{C1,3,5}$	5//0.18
$M_{b6,7}$	1/20	$M_{C2,4,6}$	20/0.18
M_{b8-10}	1/0.18	$M_{P1,3}$	1/1
$M_{b11,12}$	0.5/0.18	$M_{P2,4}$	30/0.18

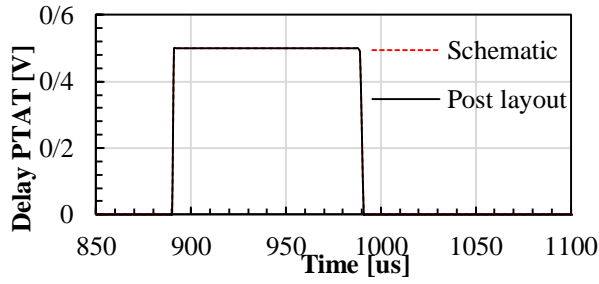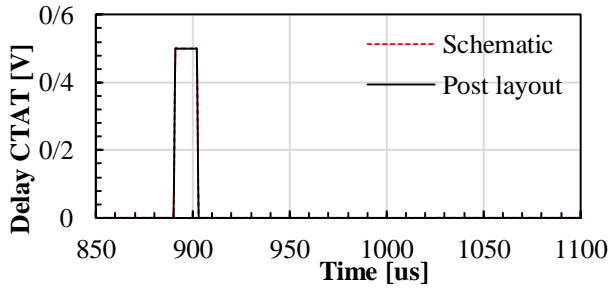Figure 5. The configuration of the proposed T-FF with GDI cell [13]

(a)

(b)

Figure 6.   The simulation results of (a) VCTAT, (b) VPTAT for temperature range of -10℃ to 20℃
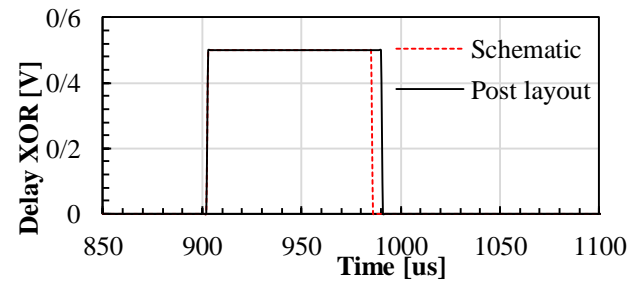
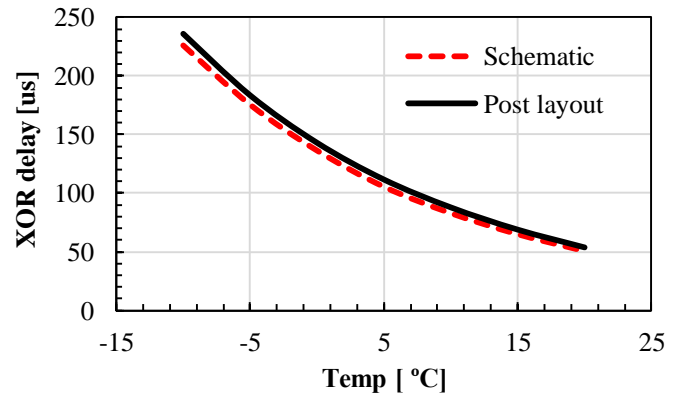Fig.7 shows the outputs of PTAT delay generator, CTAT generator and XOR at 10℃.
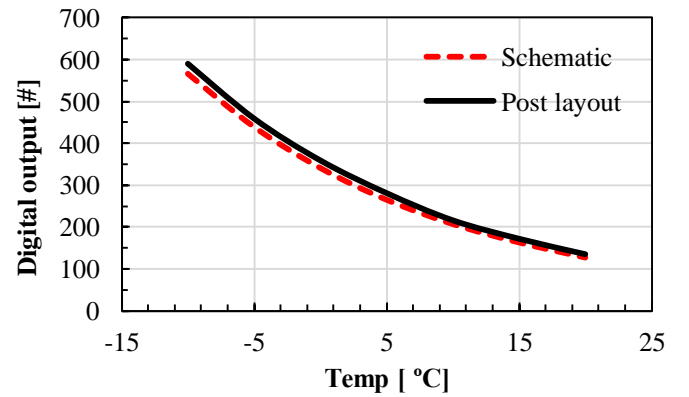

(a)

(b)

(c)

Figure 7.   (a) The PTAT generator output.(b) The CTAT generator output.
(c) The XOR output at 10℃

Based on (9), by decreasing the temperature, the pulse width is increased that its curve is shown in Fig. 8(a). Fig. 8(b) shows the quantized code of the 9-bit binary counter output with 2.5MHz clock in the temperature range from -10 ℃ to 20℃.

(a)

(b)

Figure 8.   (a) The pulse width of the modulated temperature. (b) the output of
the counter in the temperature range of -10℃ to 20℃

The paths of the delay generator, PTAT and CTAT modulated temperature signals effect on the linear behavior of the sensor. The main factors of the error in the proposed temperature sensor are the process variation and mismatch of M_{P1-4}, M_{C1-6} transistors of the sensor core and also the employed capacitors to the delay generators. The Monte Carlo simulation results for 1000 runs presented the error simulation are shown in Fig. 9.

The mean and standard deviation are 0.049 ℃ and 0.13 ℃, respectively. The layout of the proposed sensor, which is shown in Fig. 10, states 0.0125 mm² chip area.

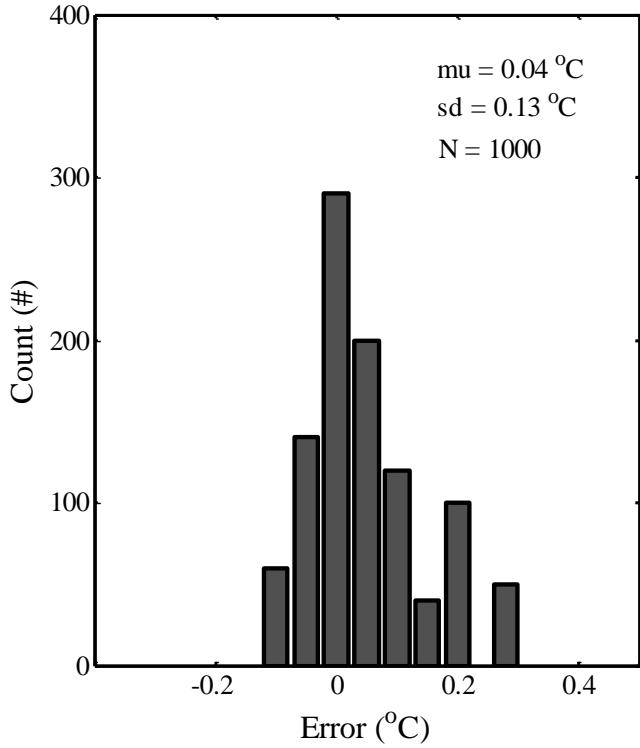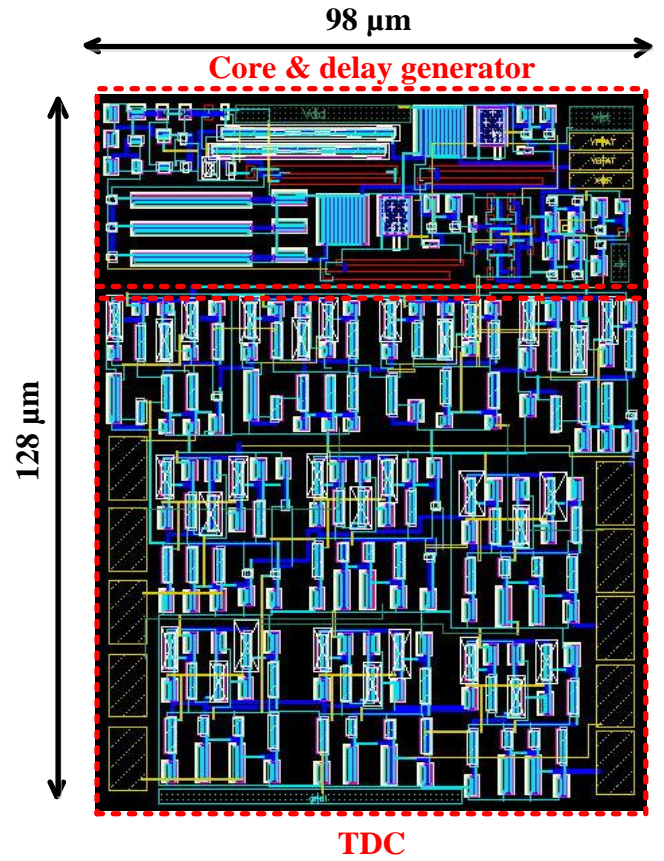Figure 9. The error in the temperature range of -10℃ to 20℃ by 1000 Monte Carlo simulation runs

Figure 10. The layout of the proposed temperature sensor

Table 2 compares the operation of the proposed temperature sensor with that of the other designed temperature sensors of the previous works. In compare with the other sensors, the chip area and the power consumption of the proposed sensor are significantly ameliorated.

Table 2. The operation comparison of the CMOS temperature sensors

Ref	Architecture Type	Process Technology [nm]	Power Consumption [μW]	Supply Voltage [V]	Temperature Range [˚C]	Area [mm²]	Error [˚C]
[2]	TDC-based	180	0.119	0.5-1	-10-30	0.0416	-0.8/+1
[3]	ADC-based	160	7.4	1.6-2	-30-125	0.12	±0.2
[4]	ADC-based	160	-	1.5-2	-55-125	0.08	±0.15
[6]	TDC-based	180	0.9	0.6-1	-20-30	-	±0.8
[8]	FDC-based	180	0.22	1	0-100	0.05	-1.6/+3
[9]	FDC-based	130	0.095	0.3	8-85	0.04	-
This work	TDC-based	180	0.112	0.5	-10-20	0.0125	-0.1/0.3

IV. Conclusion

In this paper, the low power CMOS sensor is designed in the temperature range of -10℃ to 20℃, for the purpose of temperature controlling on the food. In this design, for low power consumption, all transistors of the sensor core work in the sub-threshold region and T-FF with GDI technique is used instead of the conventional T-FF. The power dissipation of the sensor core, delay generator and digital part are 112 nW, under the condition of 0.5V supply voltage and 10℃ temperature. In addition, the simulation error is -0.1/0.3℃ for the temperature range of -10℃ to 20℃. this low power and low chip area sensor is appropriate for RFID tag applications. The proposed temperature sensor is simulated in 180nm CMOS technology with the help of Cadence software.

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